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(52) UK CL (Edition N)
H2H HAJ HBCA HBCD HBCG HBD HB8
G3U UAA9 U208 U212 U213 U301 U303 U306

(56) Documents Cited
GB 2210214 A GB 2171861 A US 5221862 A
US 5172009 A US 4827151 A US 4065711 A
S.Sivakumar,K.Natarajan,"Kalman filter based high speed meas urement and control of AC voltages(cont) for UPS applications",1993 IEEE Power Electronics Specialist s Conference Record pp907-912, (cont) Seattle,Washington,June 1993

(58) Field of Search
UK CL (Edition M) H2H HAJ
INT CL[5] G05F 1/70, H02J 9/00 9/04 9/06, H02M 1/00
ONLINE DATABASE : WPI

(54) Off-Line Uninterruptible Power Supply

(57) The UPS has circuitry arranged in a battery charger configuration in mains mode and in an inverter configuration in backup mode, the two configurations sharing a number of electrical components C5/C7, C6, D1-D4, L6/L7, 30. In the mains mode, inverse diodes D1-D4 of an inverter 28 rectify the AC mains to charge the battery 18 via a power factor corrector circuit 38 and a battery charger 44. Inductors in an inverter filter 30 aid the power factor corrector 18 in ensuring that harmonic-free high power factor AC mains current is drawn for battery charging. The power factor corrector 38 is a PWM DC-DC booster and the battery charger 44 is a buck PWM DC-DC converter providing a current-limited, regulated charging voltage. In back-up mode, the battery voltage is boosted by PWM DC-DC converter 36 before application to PWM inverter 28 via a switch 48 bypassing power factor corrector 38. A mains monitor effects a transfer between mains and back-up mode if either the mains voltage or frequency is too low or too high. Monitoring of the mains supply and control of the inverter 28 involve use of Kalman filter based DSP models.

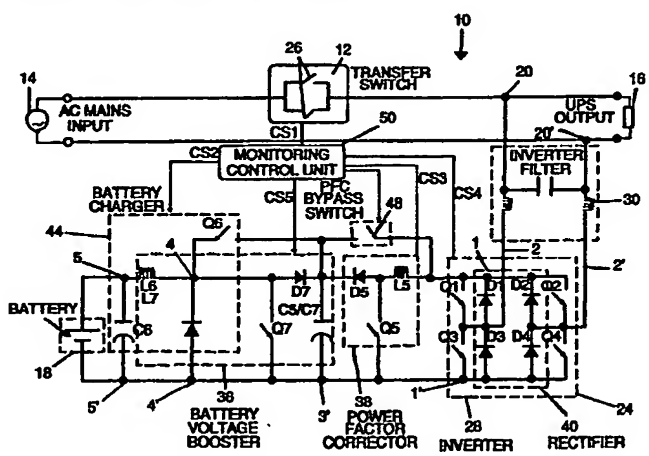


FIGURE 2A

At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.

GB 2 287 843 A

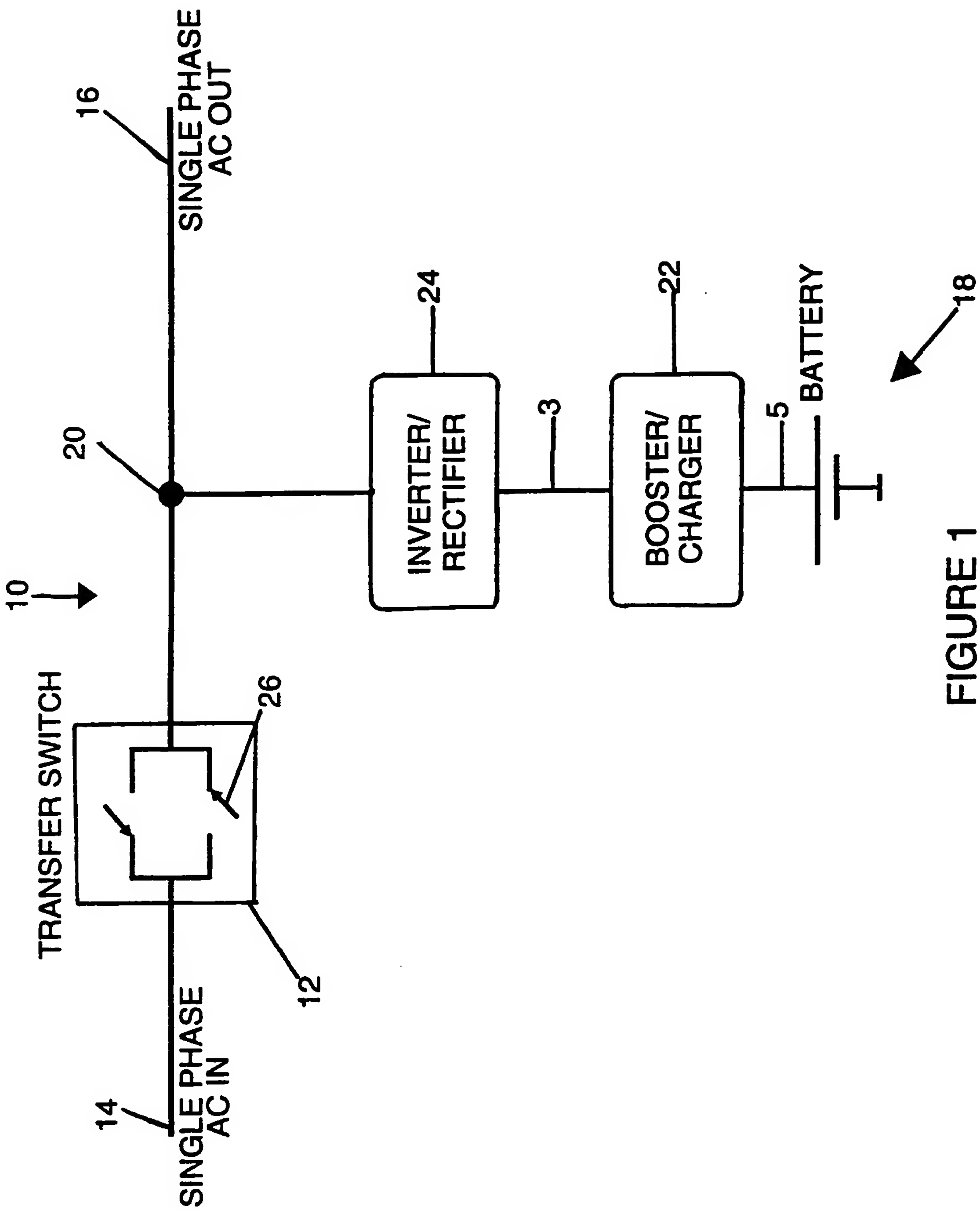

SINGLE PHASE AC OUT
16
20
10
TRANSFER SWITCH
26
12
SINGLE PHASE AC IN
14
INVERTER/ RECTIFIER
24
3
BOOSTER/ CHARGER
22
5
BATTERY
18

FIGURE 1

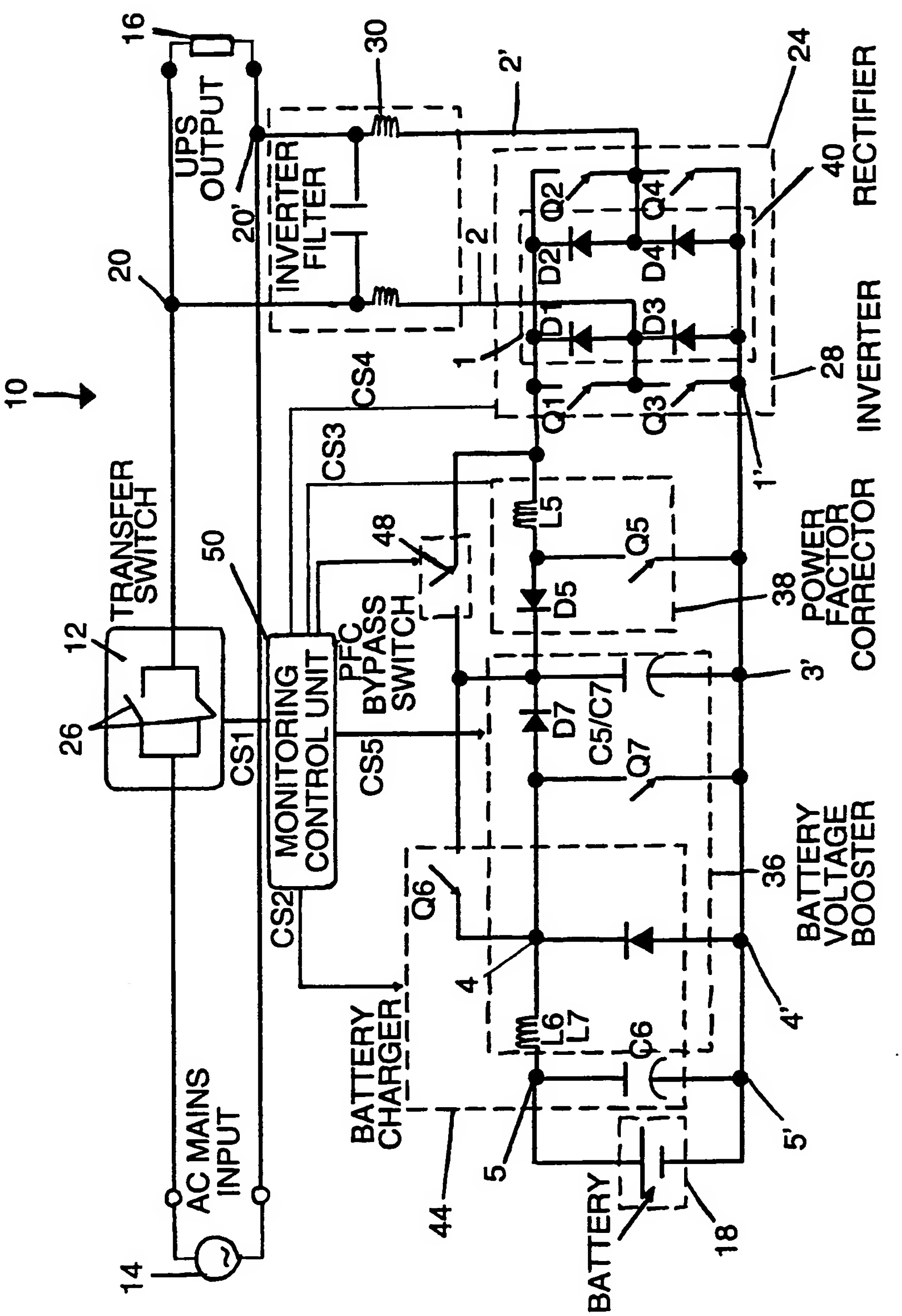
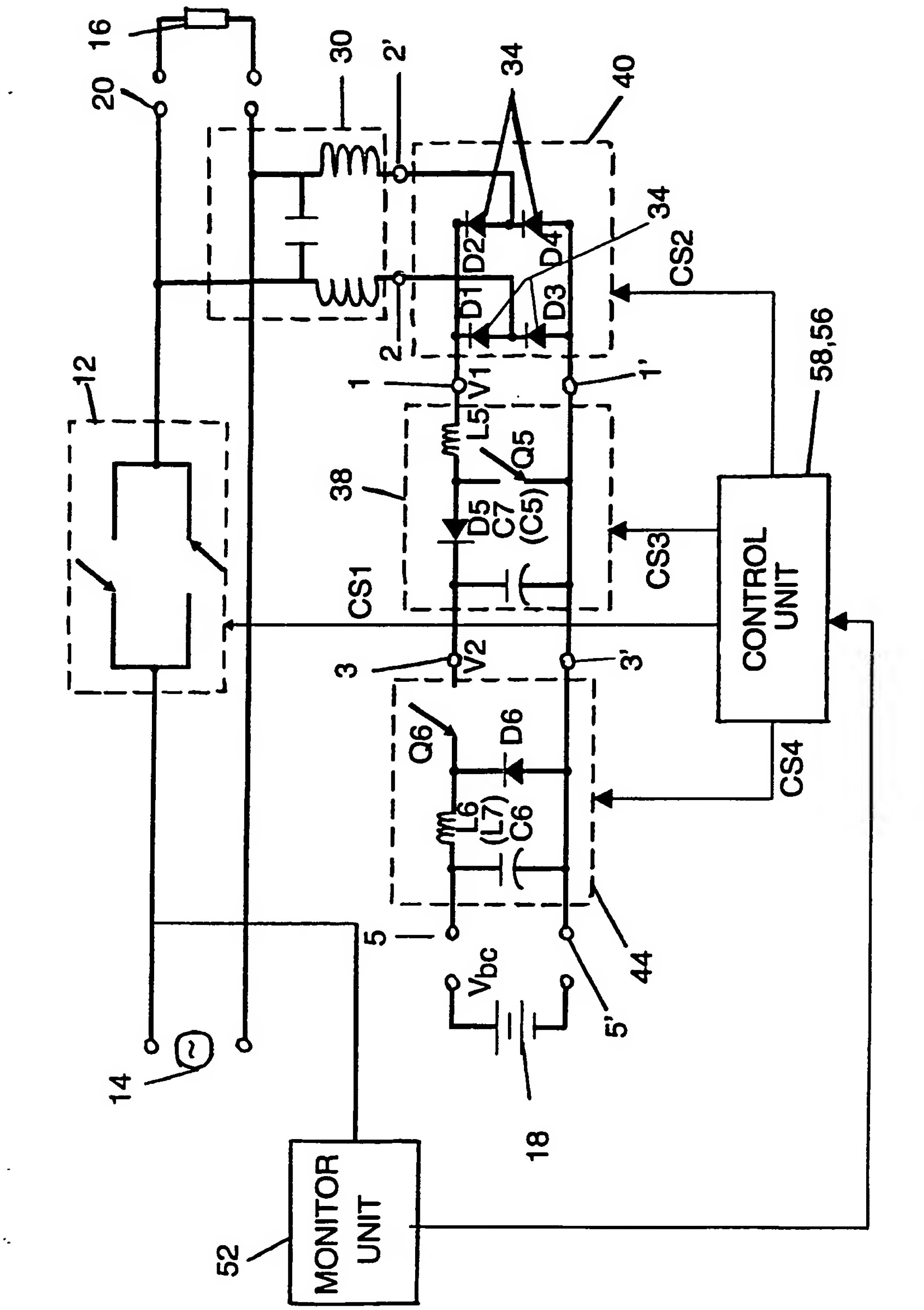
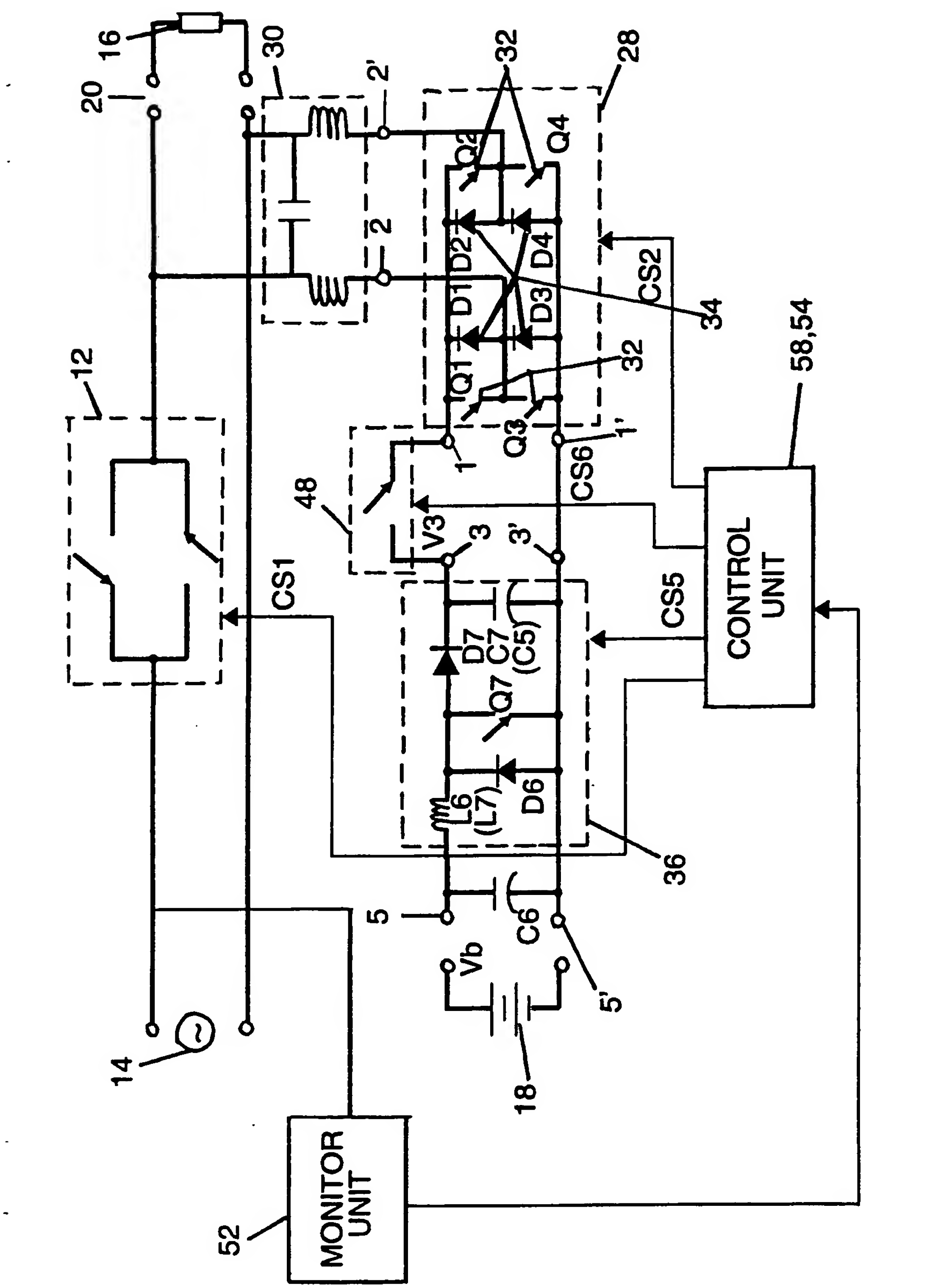

10
12
TRANSFER SWITCH
26
14
AC MAINS INPUT
16
UPS OUTPUT
20
20'
INVERTER FILTER
30
2'
2
24
RECTIFIER
40
INVERTER
28
1
1'
Q1
Q2
Q3
Q4
D1
D2
D3
D4
50
MONITORING CONTROL UNIT
CS1
CS2
CS3
CS4
CS5
48
PFC BYPASS SWITCH
L5
Q5
D5
38
POWER FACTOR CORRECTOR
3'
D7
C5/C7
Q7
36
BATTERY VOLTAGE BOOSTER
Q6
4
4'
L6
L7
C6
BATTERY CHARGER
44
5
5'
BATTERY
18

FIGURE 2A



16
20
30
2'
34
40
34
CS2
D1
D2
D3
D4
2
12
1
V1
1'
58,56
L5
Q5
38
D5
C7
(C5)
CS3
CS1
CONTROL
UNIT
3
V2
3'
Q6
D6
CS4
L6
(L7)
C6
5
44
V_{DC}
5'
14
18
MONITOR
UNIT
52

FIGURE 2B



12
14
16
18
20
28
30
32
32
34
36
48
52
58,54
CS1
CS2
CS5
CS6
V3
CONTROL UNIT
MONITOR UNIT
Q1
Q2
Q3
Q4
Q7
D1
D2
D3
D4
D6
D7
L6
(L7)
C6
C7
(C5)
Vb
1
1'
2
2'
3
3'
5
5'

FIGURE 2C

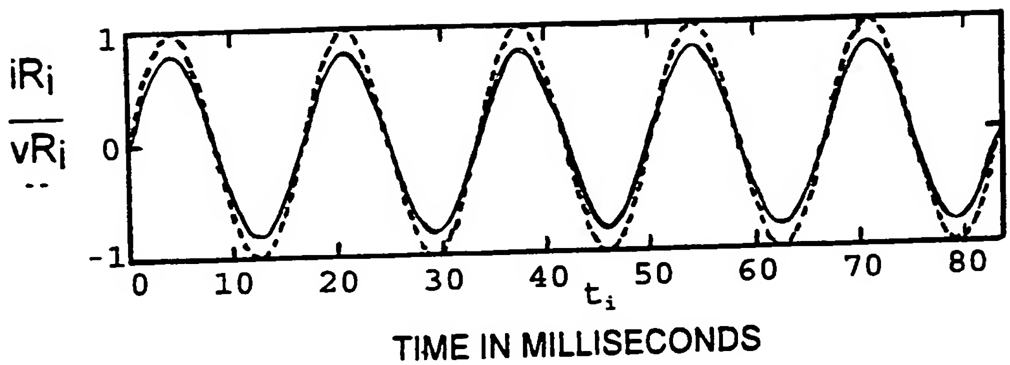


FIGURE 3

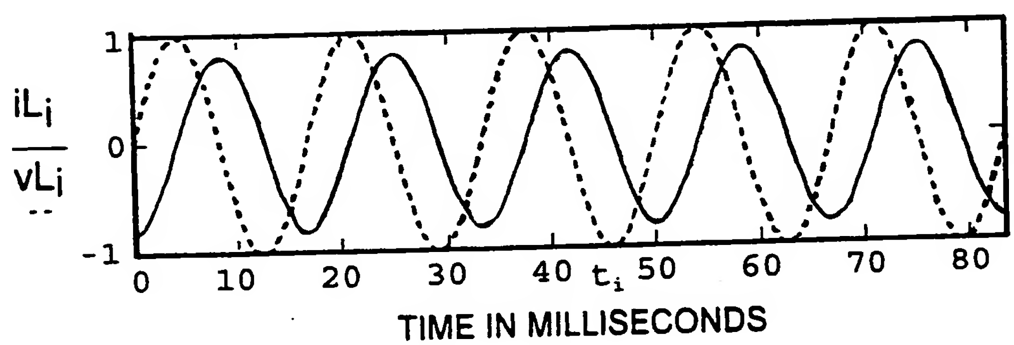


FIGURE 4

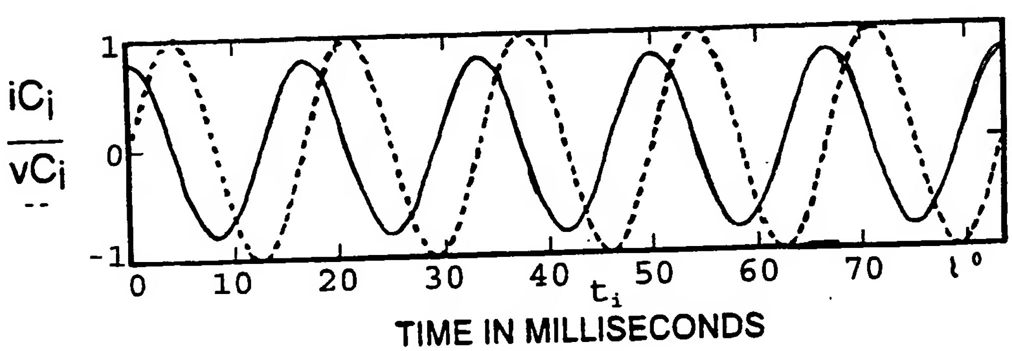


FIGURE 5

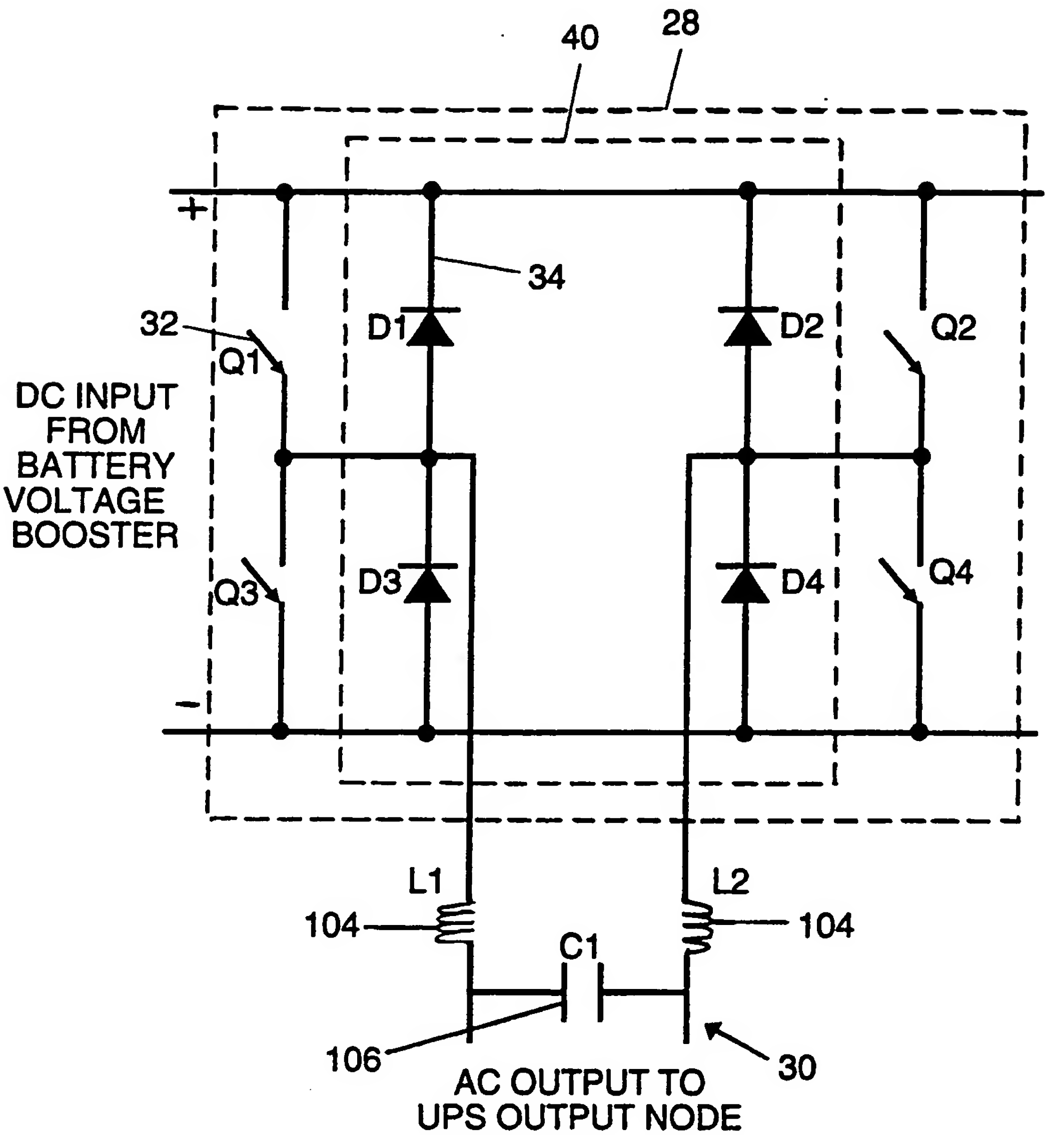
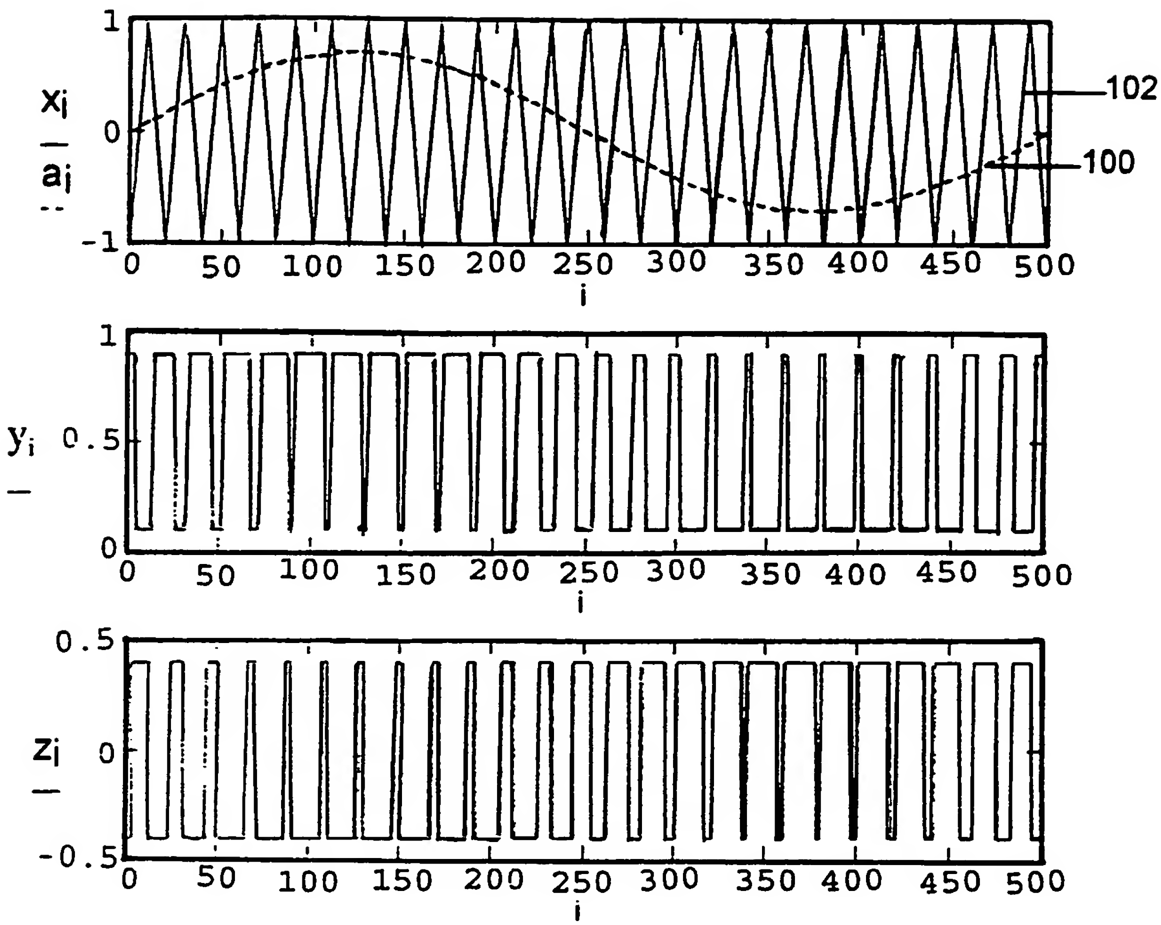

40
28
+
34
32
D1
D2
Q2
Q1
DC INPUT
FROM
BATTERY
VOLTAGE
BOOSTER
D3
D4
Q4
Q3
-
L1
L2
104
104
C1
106
30
AC OUTPUT TO
UPS OUTPUT NODE

FIGURE 6

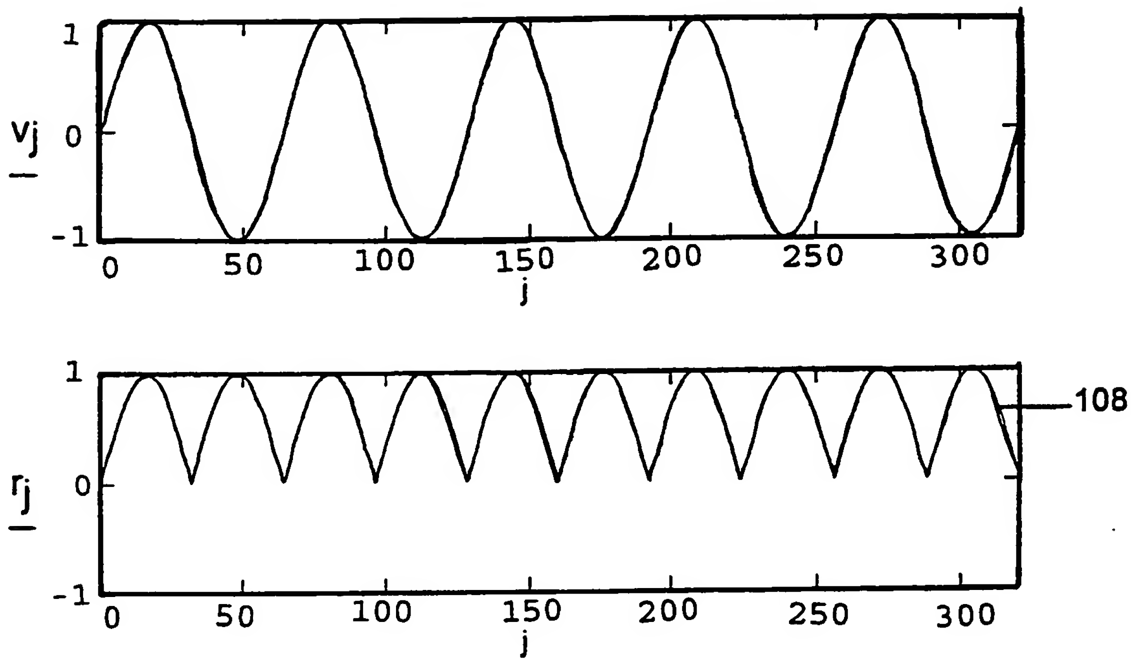


TOP TRACES: TRIANGULAR CARRIER WAVE AND MODULATING SINEWAVE

MIDDLE TRACE: PWM+

BOTTOM TRACE: PWM-

FIGURE 7



TOP TRACE (v): RECTIFIER INPUT VOLTAGE

BOTTOM TRACE (r): RECTIFIER OUTPUT VOLTAGE WAVEFORM

FIGURE 8

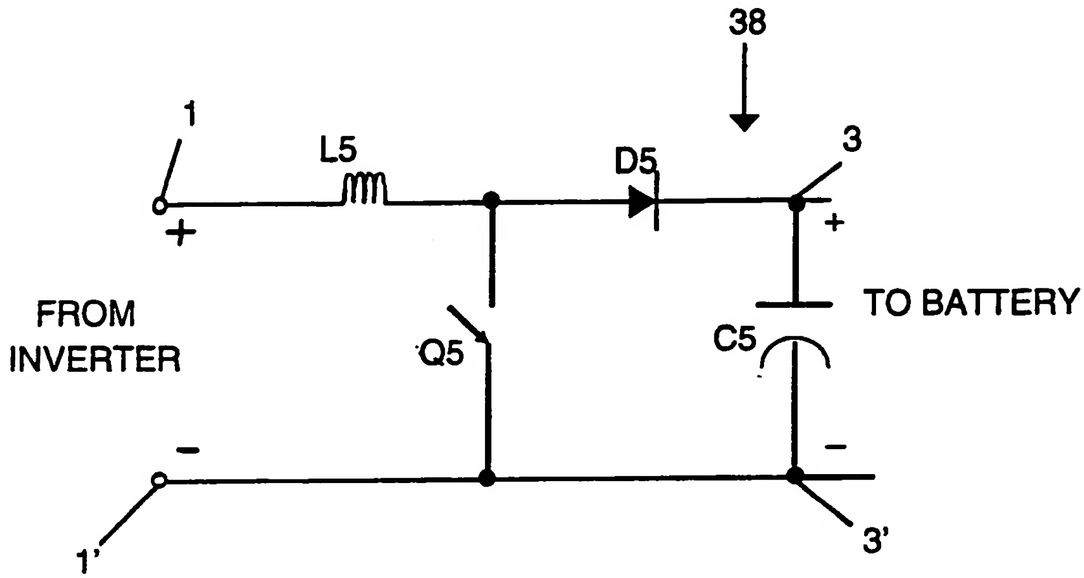


FIGURE 9

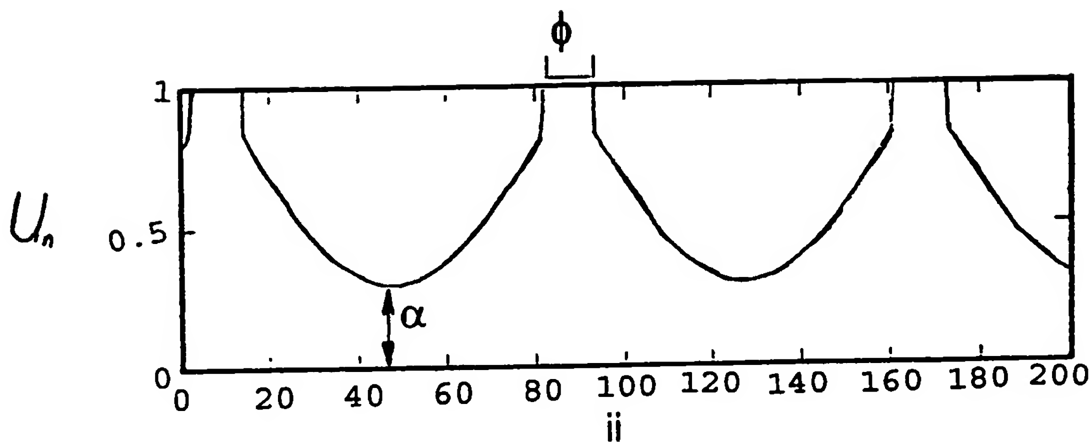


FIGURE 10

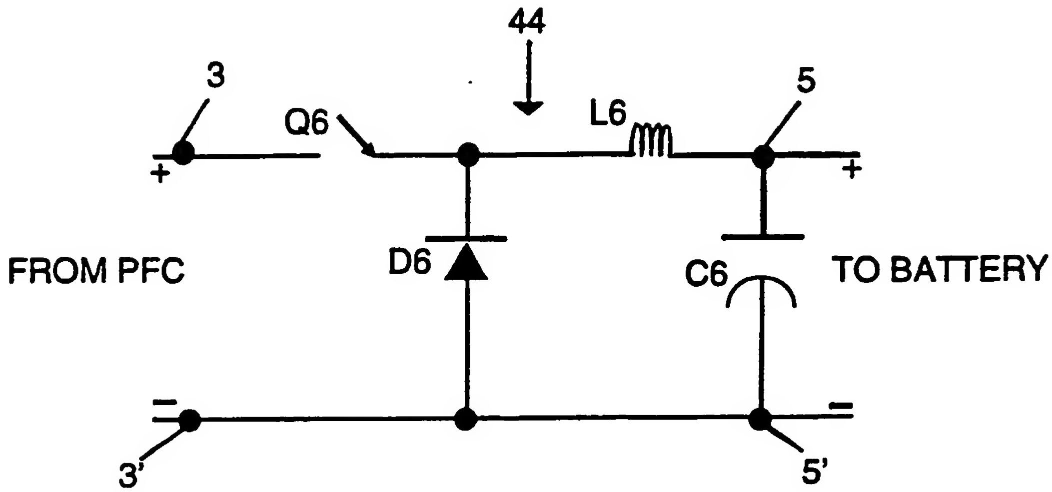


FIGURE 11

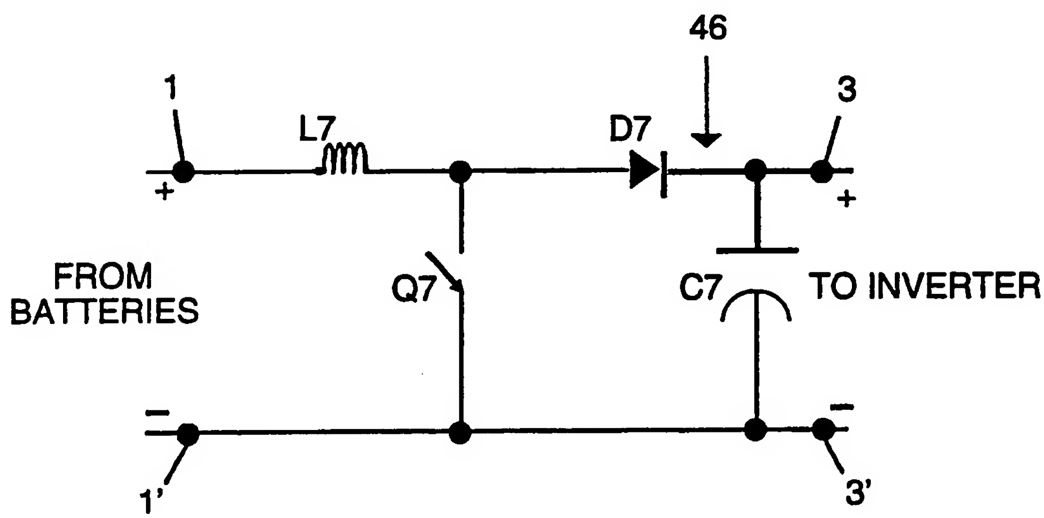


FIGURE 12

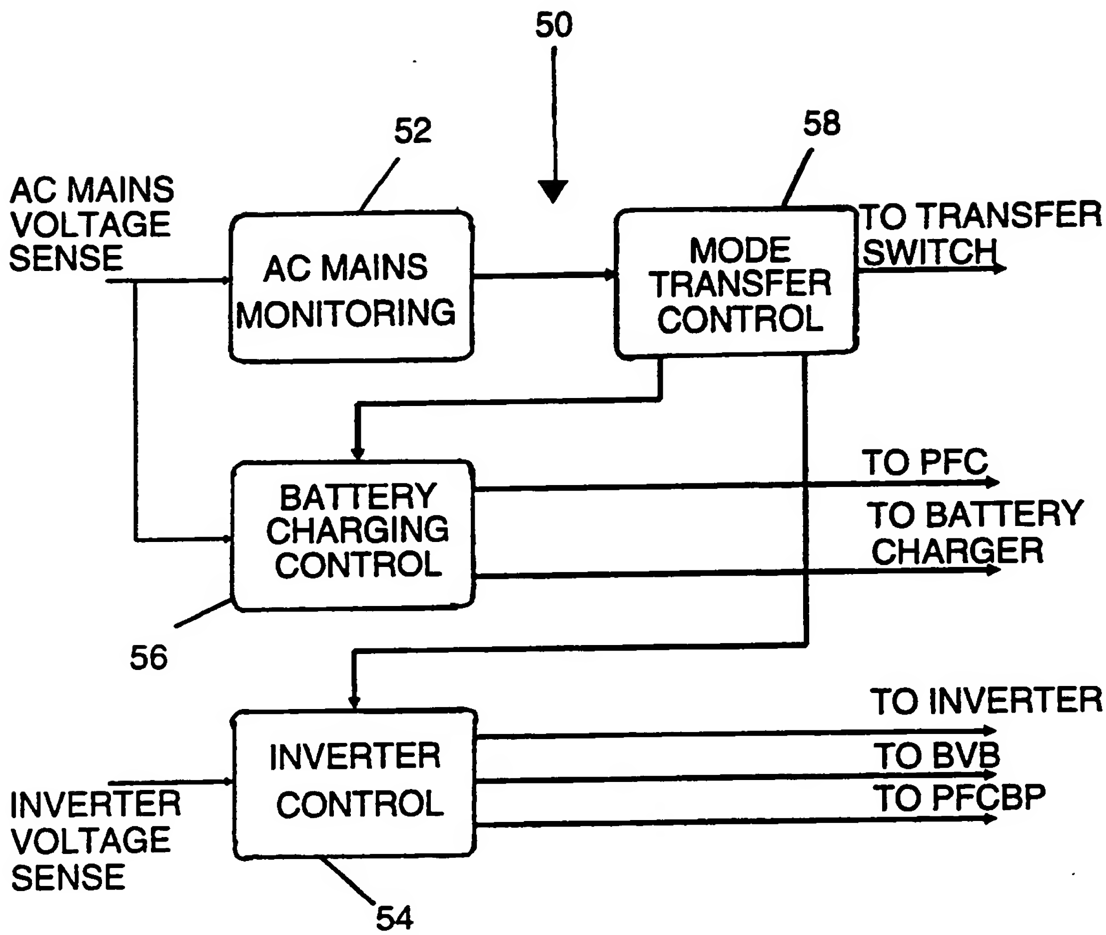

50
52
58
AC MAINS
VOLTAGE
SENSE
AC MAINS
MONITORING
MODE
TRANSFER
CONTROL
TO TRANSFER
SWITCH
BATTERY
CHARGING
CONTROL
TO PFC
TO BATTERY
CHARGER
56
INVERTER
CONTROL
TO INVERTER
TO BVB
TO PFCBP
INVERTER
VOLTAGE
SENSE
54

FIGURE 13

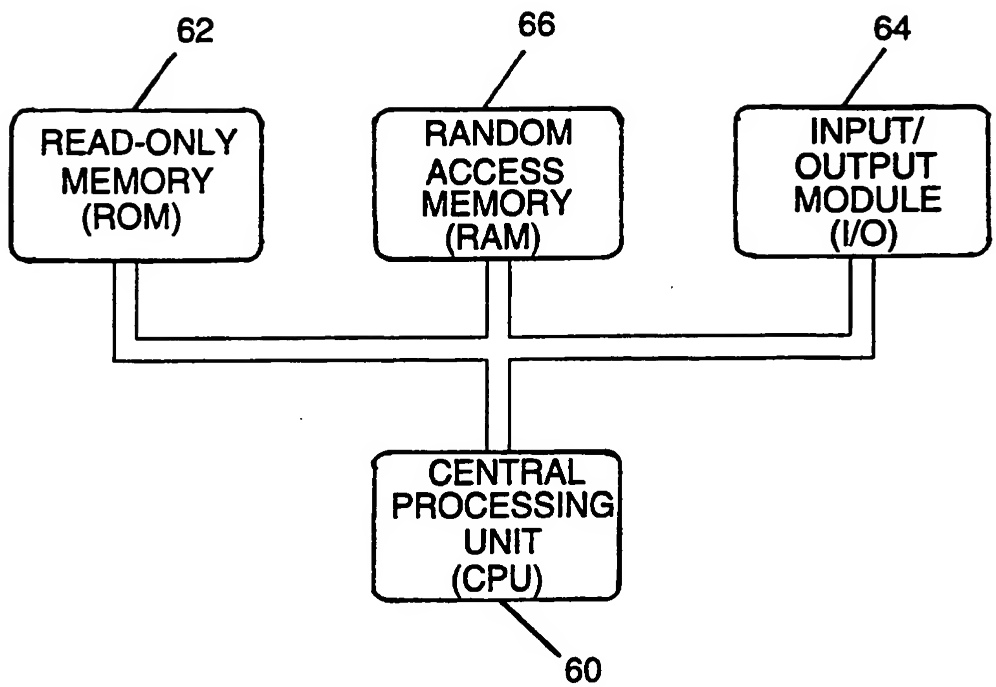

62
66
64
READ-ONLY MEMORY (ROM)
RANDOM ACCESS MEMORY (RAM)
INPUT/ OUTPUT MODULE (I/O)
CENTRAL PROCESSING UNIT (CPU)
60

FIGURE 14

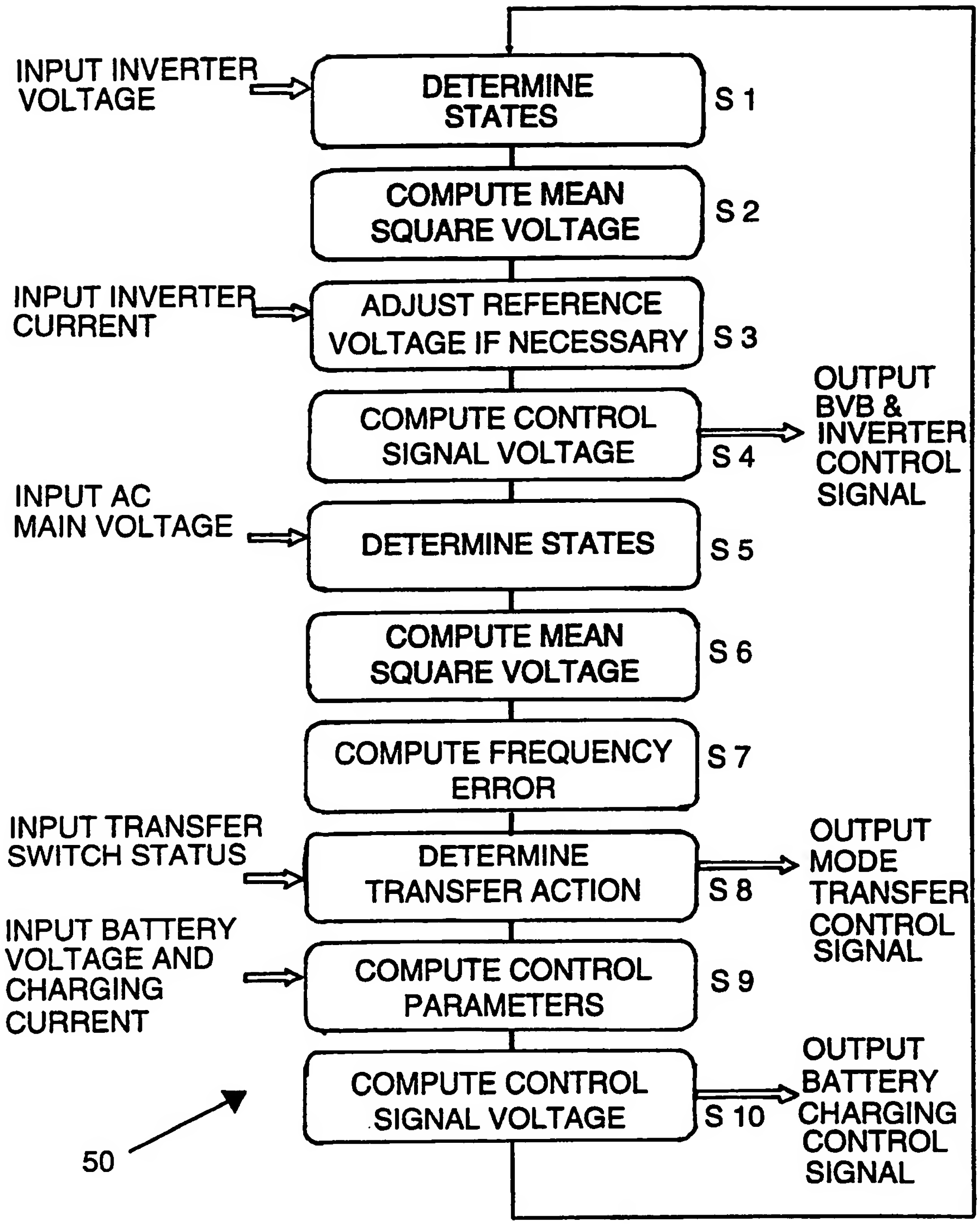

INPUT INVERTER VOLTAGE
DETERMINE STATES
S 1
COMPUTE MEAN SQUARE VOLTAGE
S 2
INPUT INVERTER CURRENT
ADJUST REFERENCE VOLTAGE IF NECESSARY
S 3
COMPUTE CONTROL SIGNAL VOLTAGE
S 4
OUTPUT BVB & INVERTER CONTROL SIGNAL
INPUT AC MAIN VOLTAGE
DETERMINE STATES
S 5
COMPUTE MEAN SQUARE VOLTAGE
S 6
COMPUTE FREQUENCY ERROR
S 7
INPUT TRANSFER SWITCH STATUS
DETERMINE TRANSFER ACTION
S 8
OUTPUT MODE TRANSFER CONTROL SIGNAL
INPUT BATTERY VOLTAGE AND CHARGING CURRENT
COMPUTE CONTROL PARAMETERS
S 9
COMPUTE CONTROL SIGNAL VOLTAGE
S 10
OUTPUT BATTERY CHARGING CONTROL SIGNAL
50

FIGURE 15

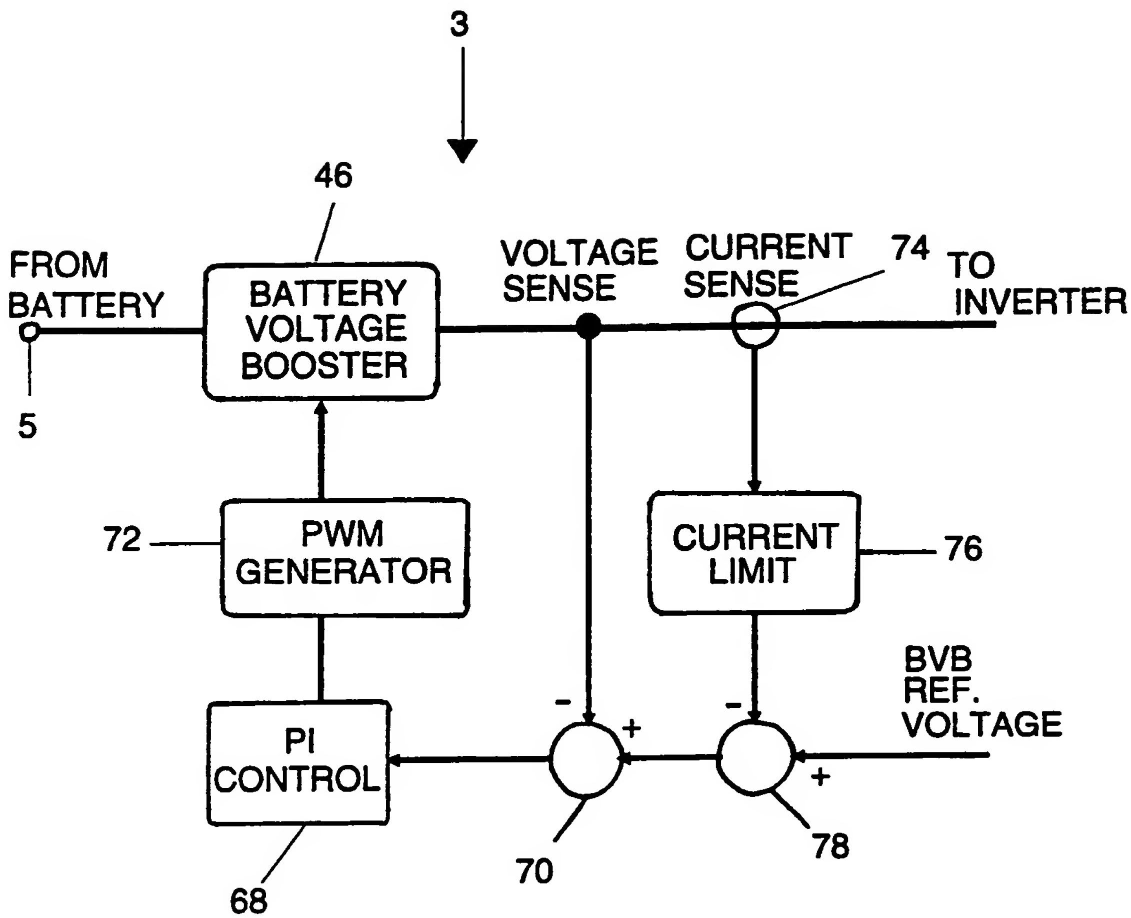
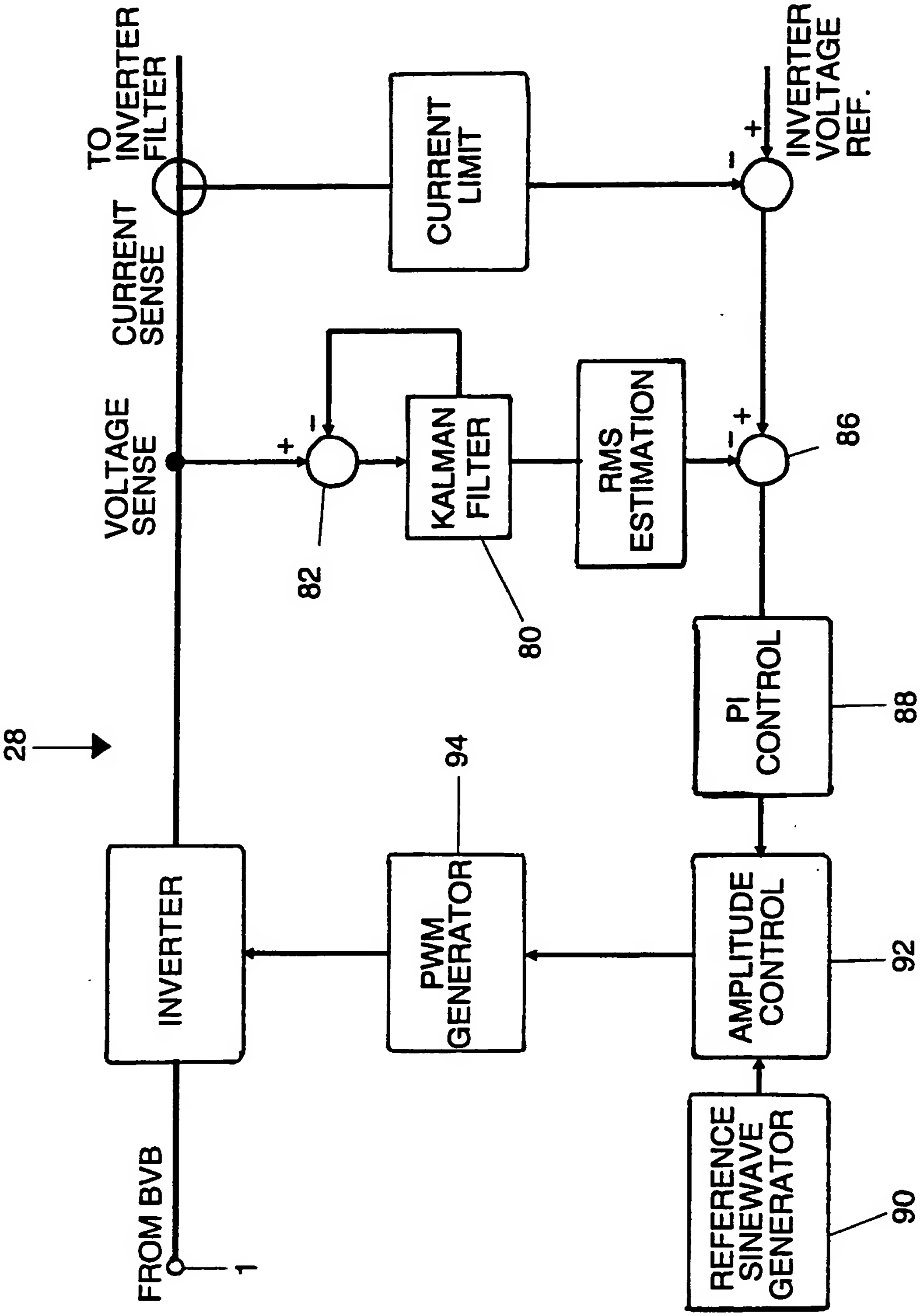

3
46
FROM
BATTERY
5
BATTERY
VOLTAGE
BOOSTER
VOLTAGE
SENSE
CURRENT
SENSE
74
TO
INVERTER
72
PWM
GENERATOR
CURRENT
LIMIT
76
BVB
REF.
VOLTAGE
PI
CONTROL
-
+
-
+
68
70
78

FIGURE 16



TO INVERTER FILTER
CURRENT SENSE
VOLTAGE SENSE
FROM BVB
1
28
INVERTER
CURRENT LIMIT
KALMAN FILTER
RMS ESTIMATION
PI CONTROL
AMPLITUDE CONTROL
REFERENCE SINEWAVE GENERATOR
PWM GENERATOR
INVERTER VOLTAGE REF.
+
-
82
80
86
88
92
90
94

FIGURE 17

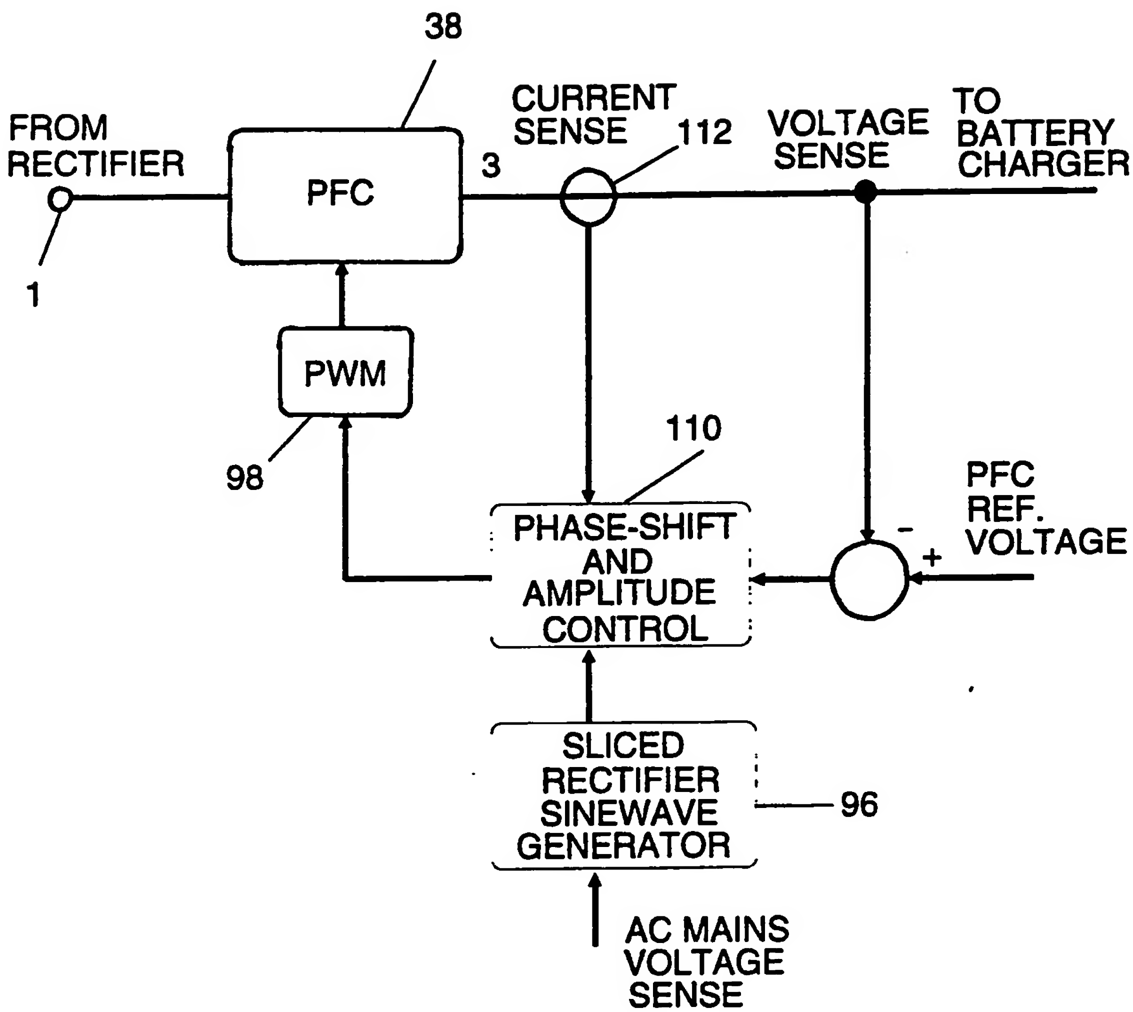

38
FROM
RECTIFIER
1
PFC
3
CURRENT
SENSE
112
VOLTAGE
SENSE
TO
BATTERY
CHARGER
PWM
98
110
PHASE-SHIFT
AND
AMPLITUDE
CONTROL
-
+
PFC
REF.
VOLTAGE
SLICED
RECTIFIER
SINEWAVE
GENERATOR
96
AC MAINS
VOLTAGE
SENSE

FIGURE 18

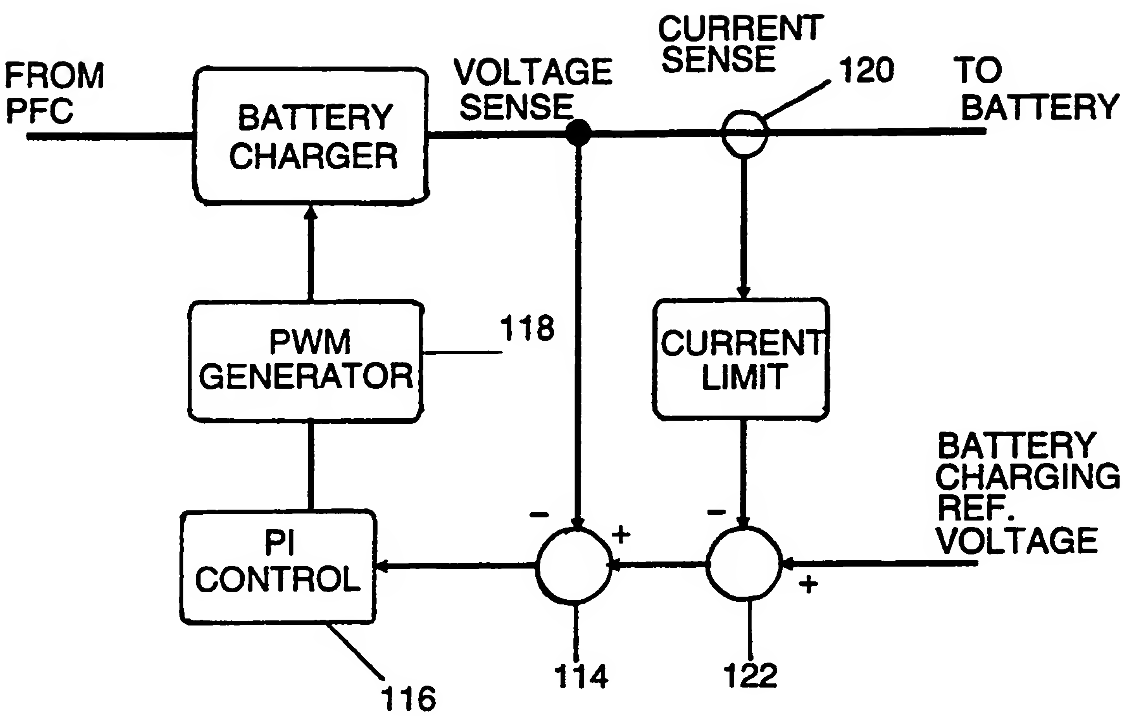

FROM
PFC
BATTERY
CHARGER
VOLTAGE
SENSE
CURRENT
SENSE
120
TO
BATTERY
PWM
GENERATOR
118
CURRENT
LIMIT
BATTERY
CHARGING
REF.
VOLTAGE
PI
CONTROL
–
+
–
+
116
114
122

FIGURE 19

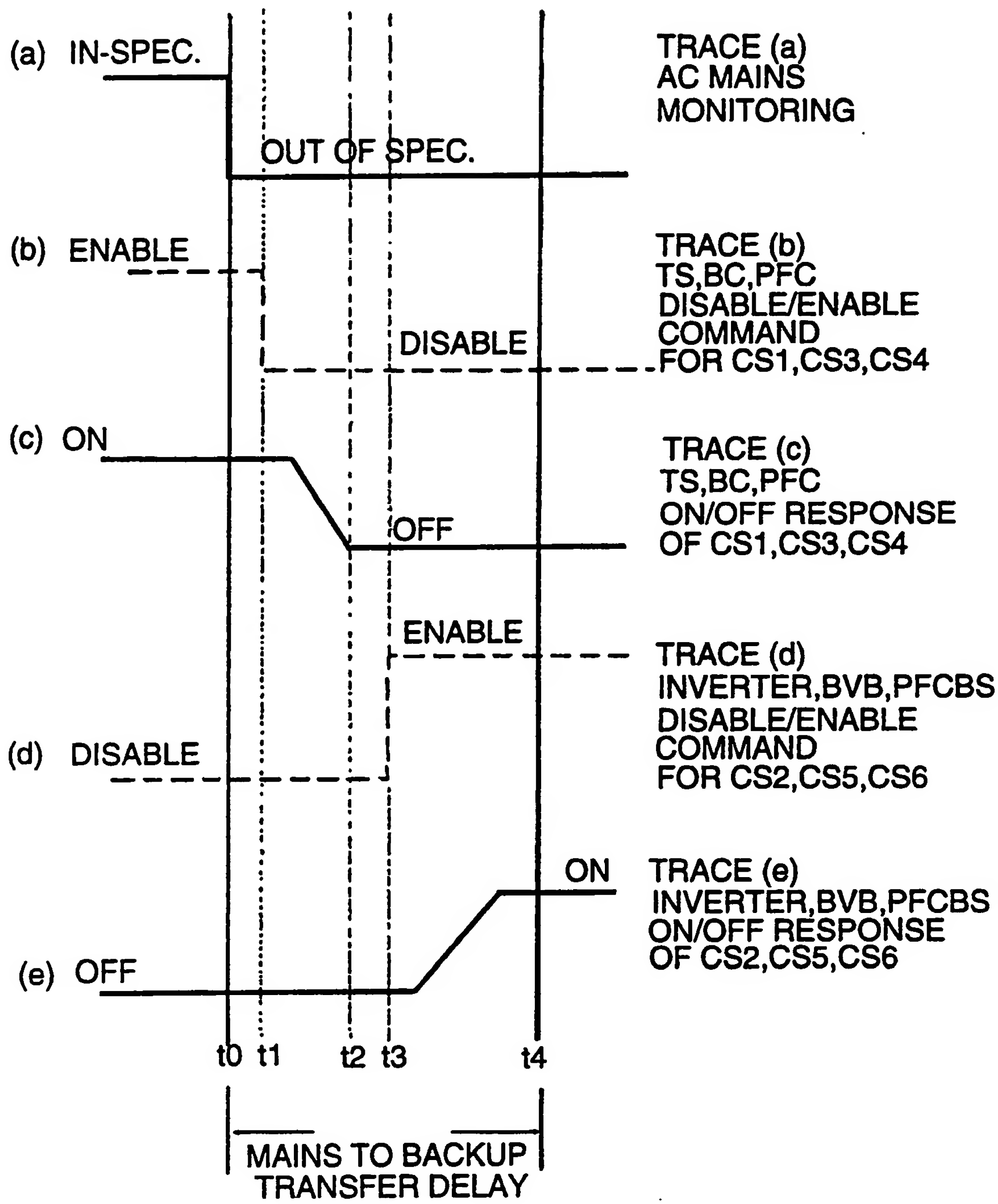

(a) IN-SPEC.
OUT OF SPEC.
TRACE (a) AC MAINS MONITORING
(b) ENABLE
DISABLE
TRACE (b) TS,BC,PFC DISABLE/ENABLE COMMAND FOR CS1,CS3,CS4
(c) ON
OFF
TRACE (c) TS,BC,PFC ON/OFF RESPONSE OF CS1,CS3,CS4
ENABLE
(d) DISABLE
TRACE (d) INVERTER,BVB,PFCBS DISABLE/ENABLE COMMAND FOR CS2,CS5,CS6
ON
(e) OFF
TRACE (e) INVERTER,BVB,PFCBS ON/OFF RESPONSE OF CS2,CS5,CS6
t0 t1 t2 t3 t4
MAINS TO BACKUP TRANSFER DELAY

FIGURE 20

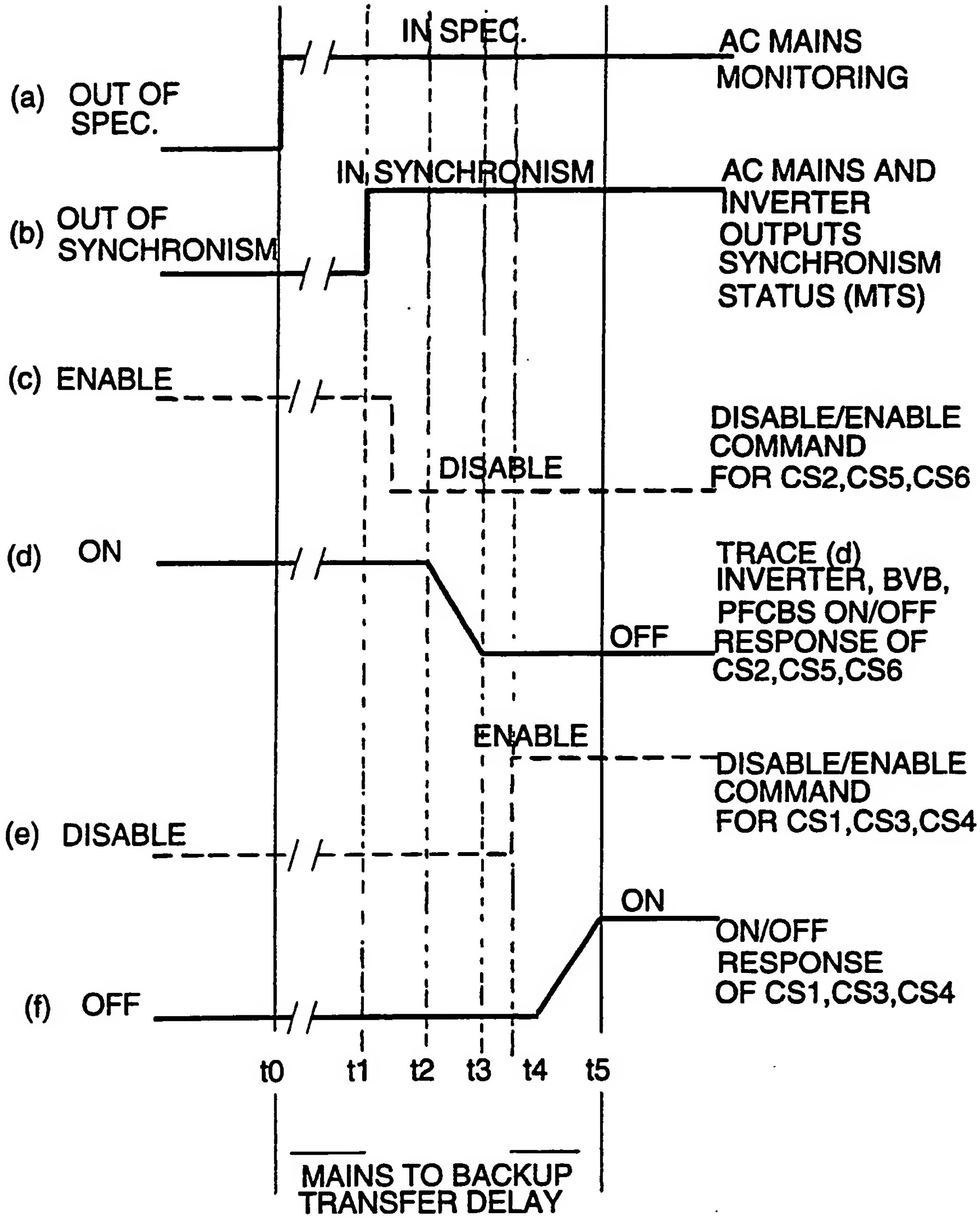

IN SPEC.
AC MAINS MONITORING
(a) OUT OF SPEC.
IN SYNCHRONISM
AC MAINS AND INVERTER OUTPUTS SYNCHRONISM STATUS (MTS)
(b) OUT OF SYNCHRONISM
(c) ENABLE
DISABLE
DISABLE/ENABLE COMMAND FOR CS2,CS5,CS6
(d) ON
OFF
TRACE (d) INVERTER, BVB, PFCBS ON/OFF RESPONSE OF CS2,CS5,CS6
ENABLE
DISABLE/ENABLE COMMAND FOR CS1,CS3,CS4
(e) DISABLE
ON
ON/OFF RESPONSE OF CS1,CS3,CS4
(f) OFF
t0 t1 t2 t3 t4 t5
MAINS TO BACKUP TRANSFER DELAY

FIGURE 21

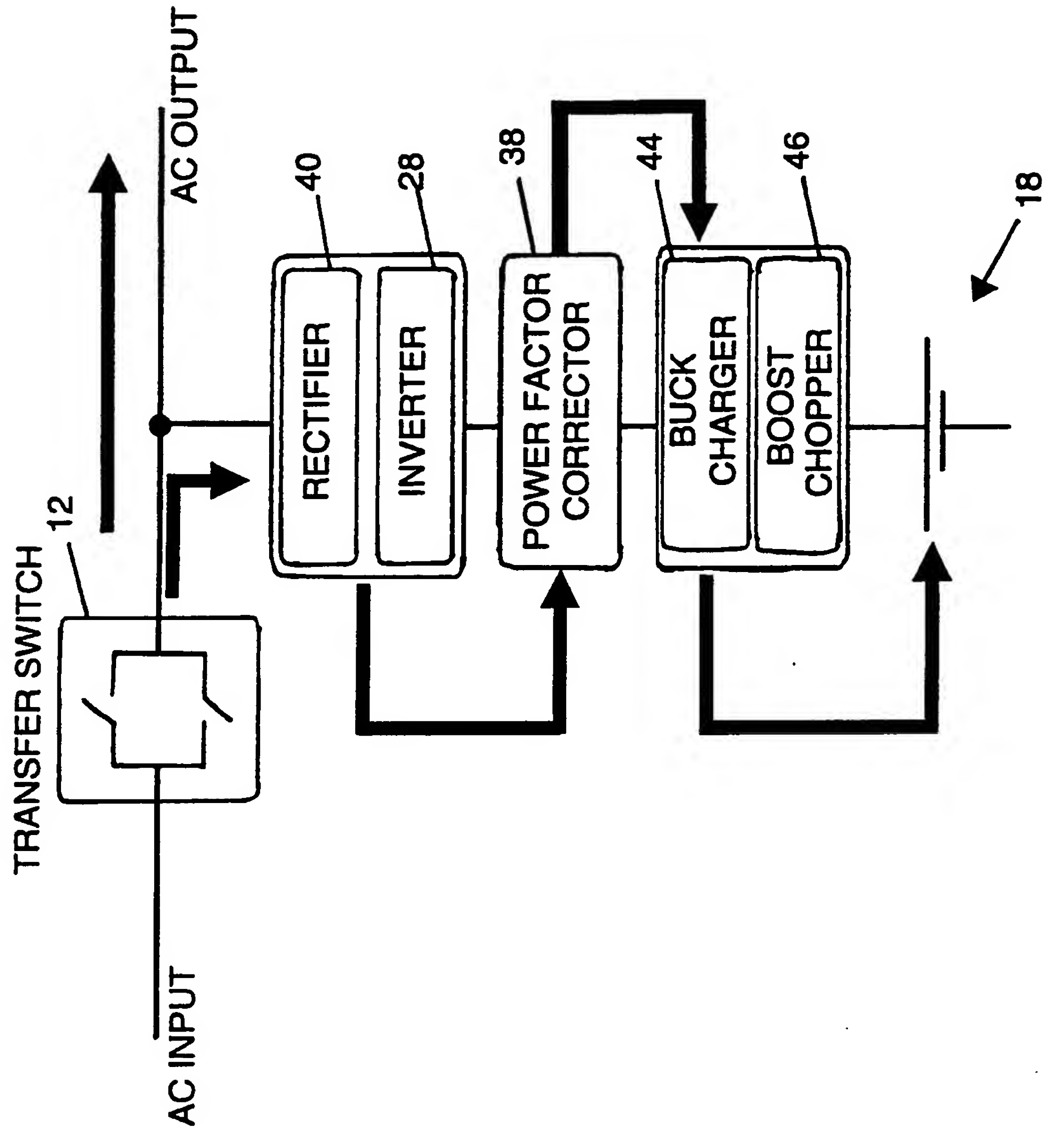

TRANSFER SWITCH
12
AC INPUT
AC OUTPUT
40
28
RECTIFIER
INVERTER
38
POWER FACTOR CORRECTOR
44
46
BUCK CHARGER
BOOST CHOPPER
18

FIGURE 22

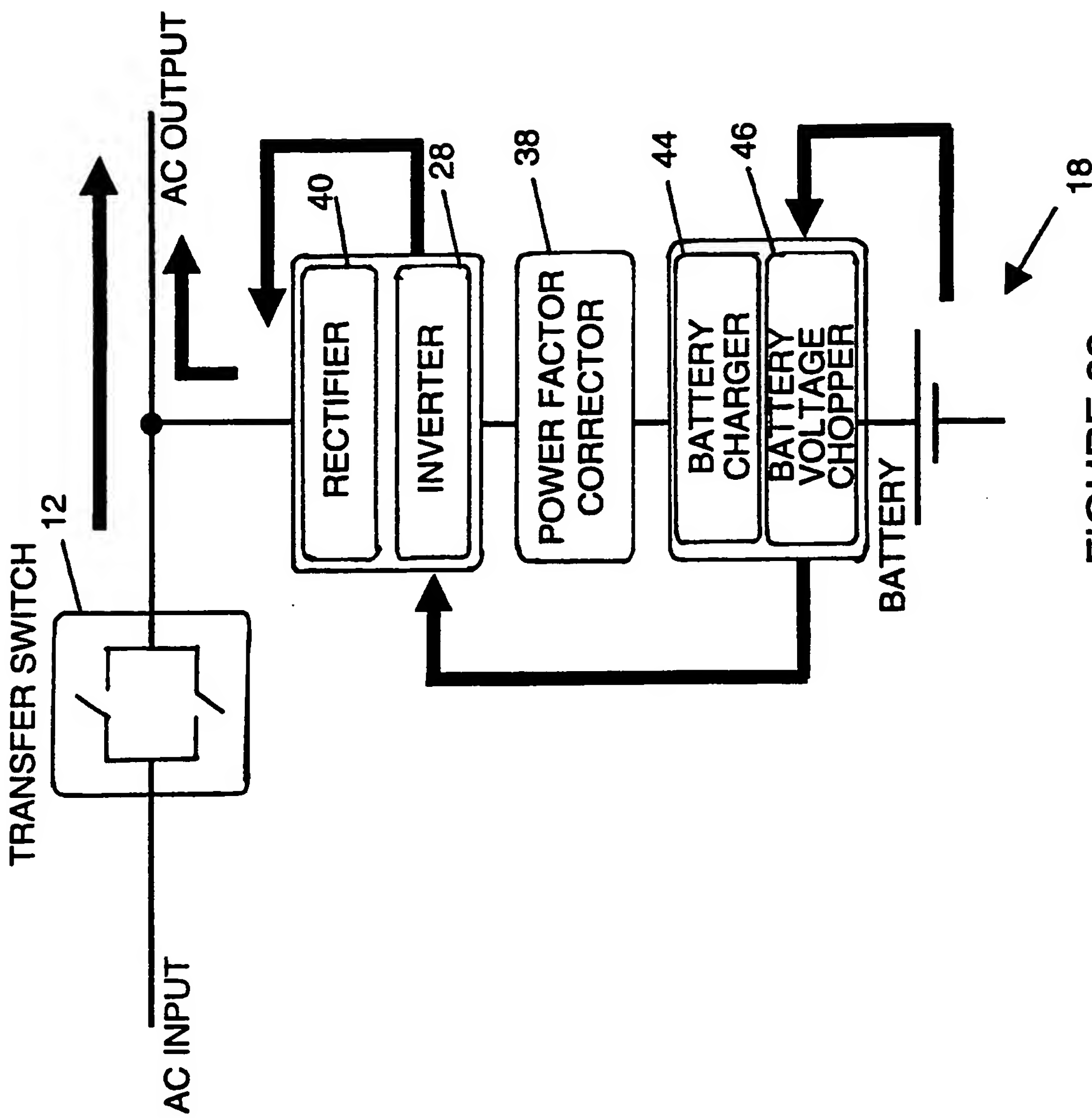
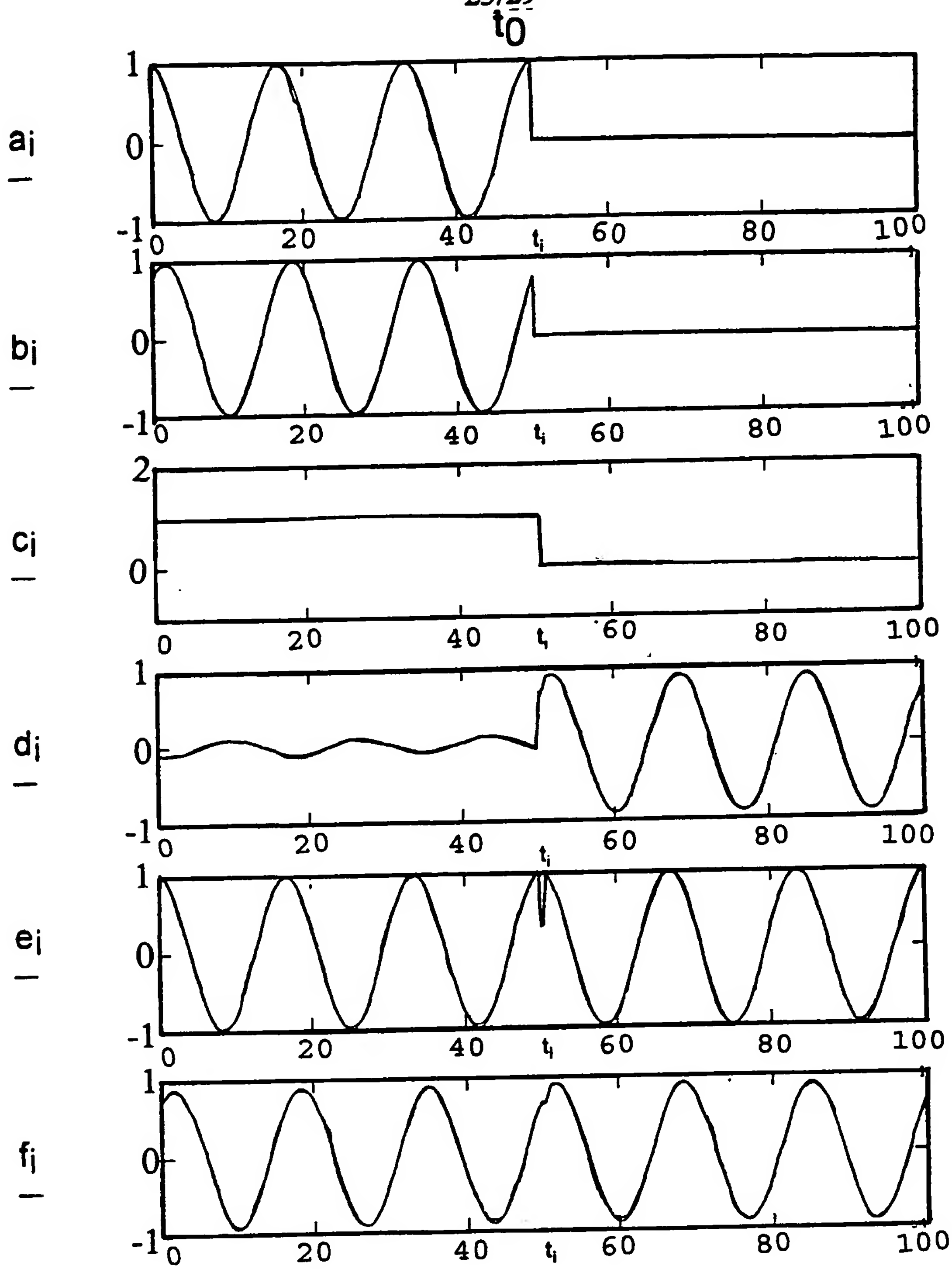
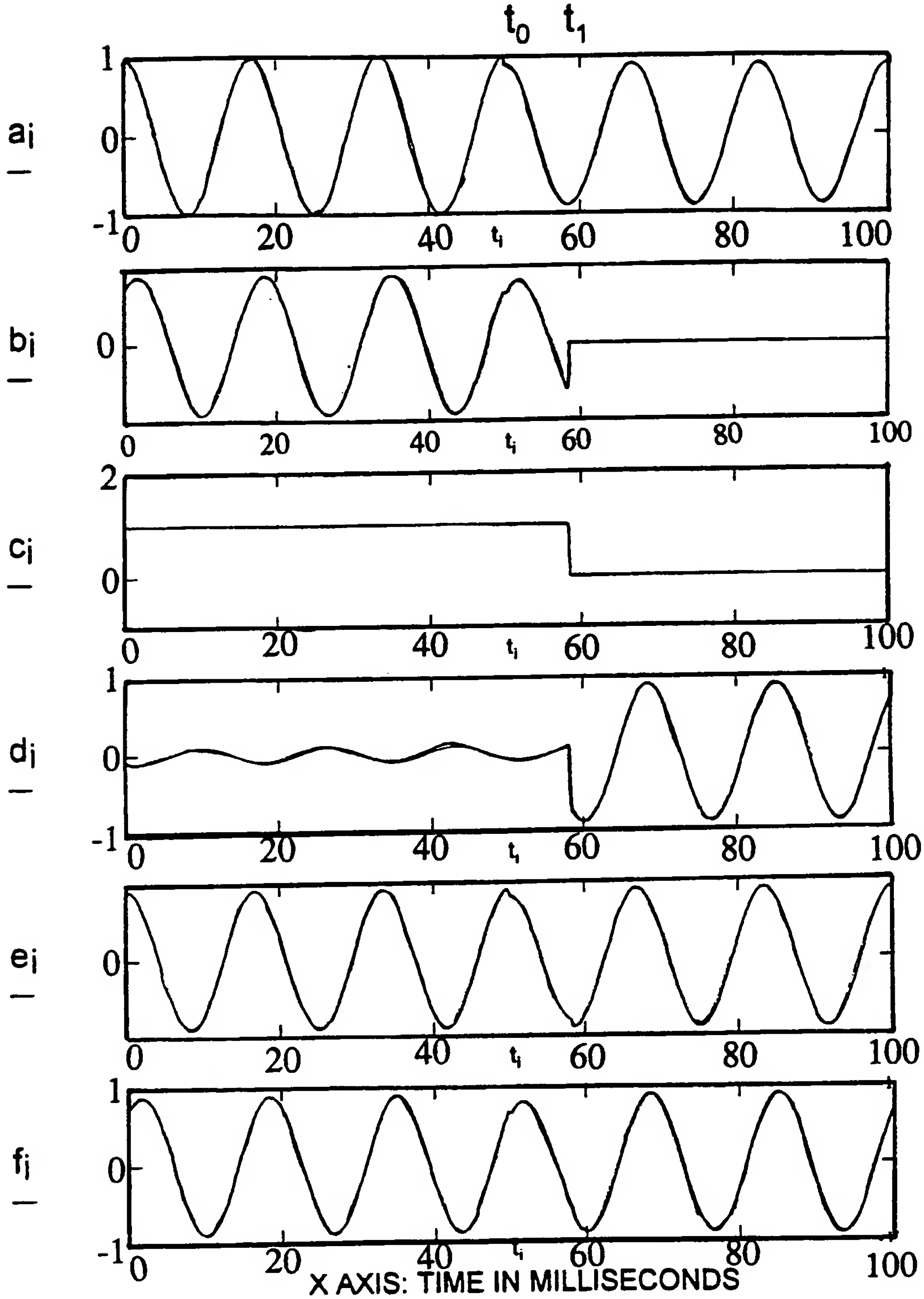

AC INPUT
TRANSFER SWITCH
12
AC OUTPUT
40
RECTIFIER
28
INVERTER
38
POWER FACTOR CORRECTOR
44
BATTERY CHARGER
46
BATTERY VOLTAGE CHOPPER
BATTERY
18

FIGURE 23



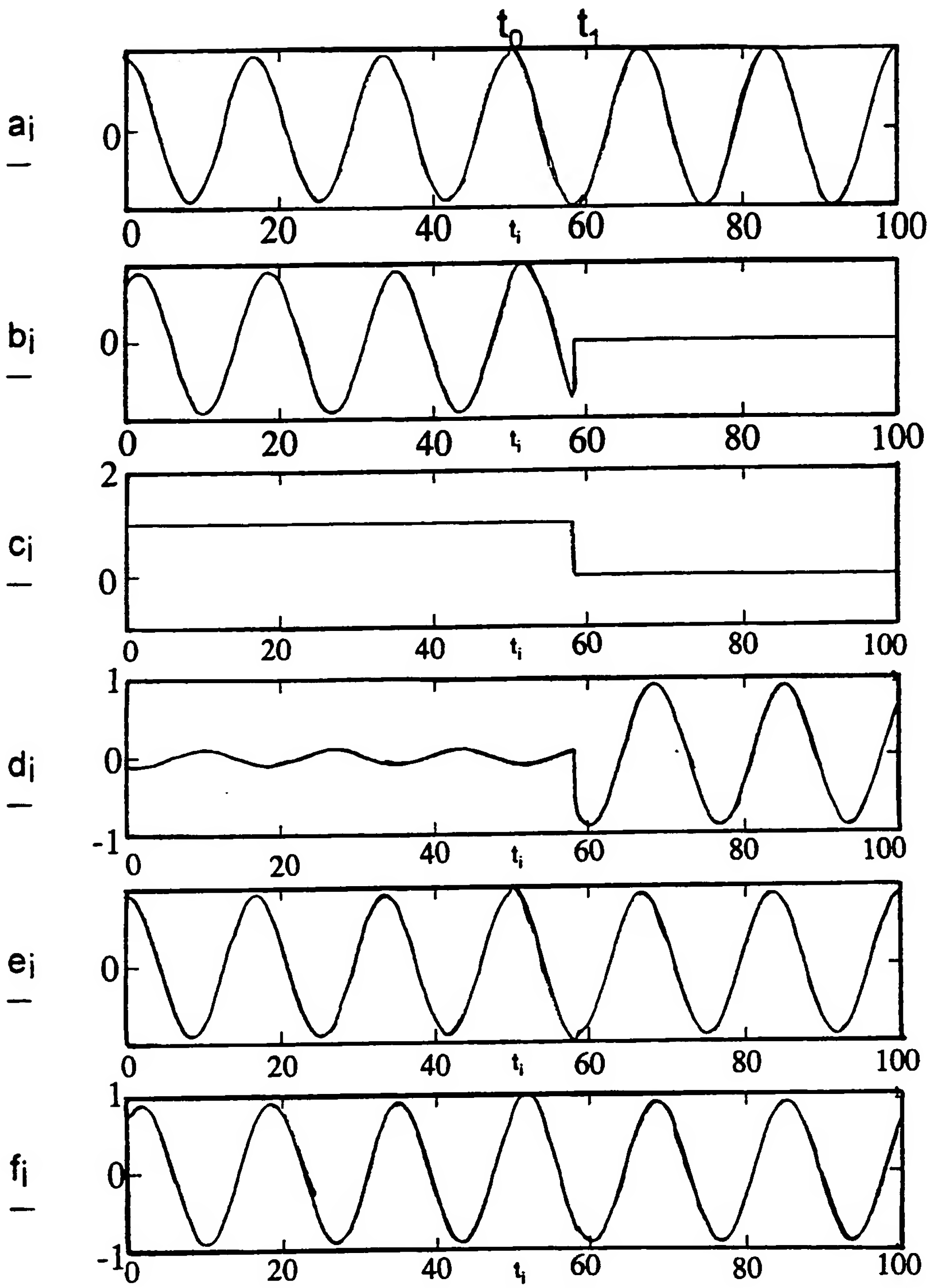
X AXIS: TIME IN MILLISECONDS

FIGURE 24



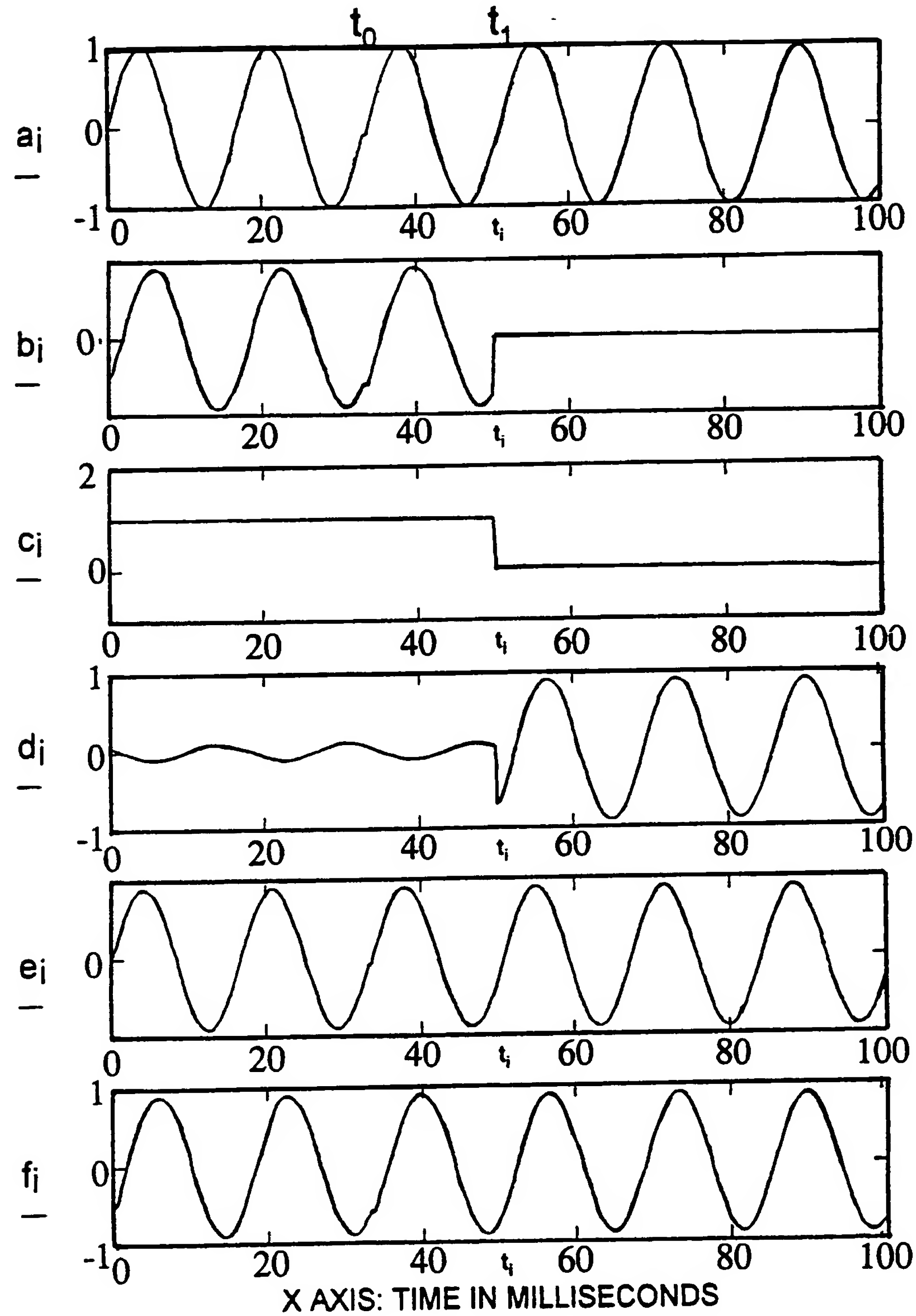
t_0 t_1
a_i
b_i
c_i
d_i
e_i
f_i
1
0
-1
2
0
20
40
60
80
100
t_i
X AXIS: TIME IN MILLISECONDS

FIGURE 25



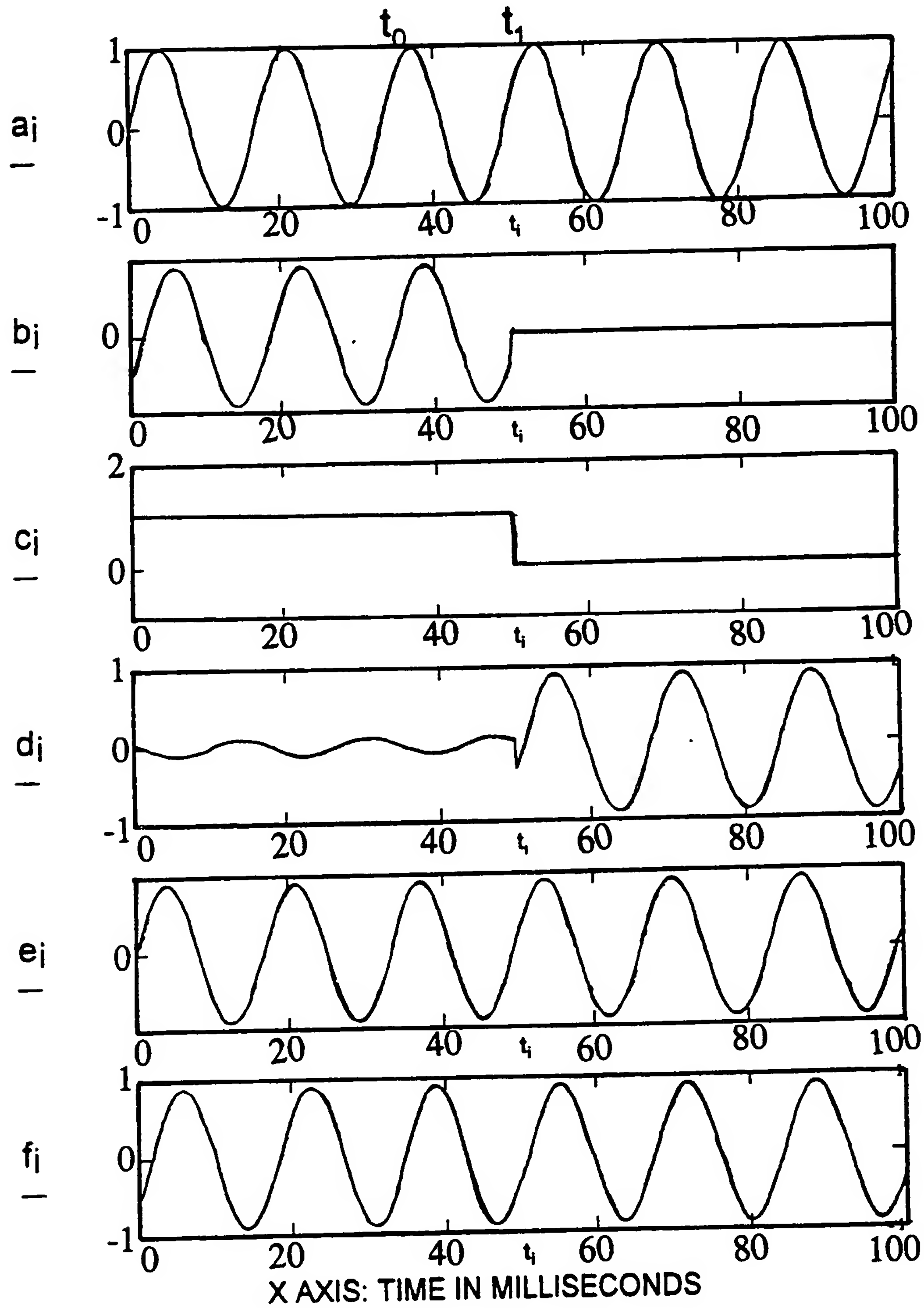
X AXIS: TIME IN MILLISECONDS

FIGURE 26



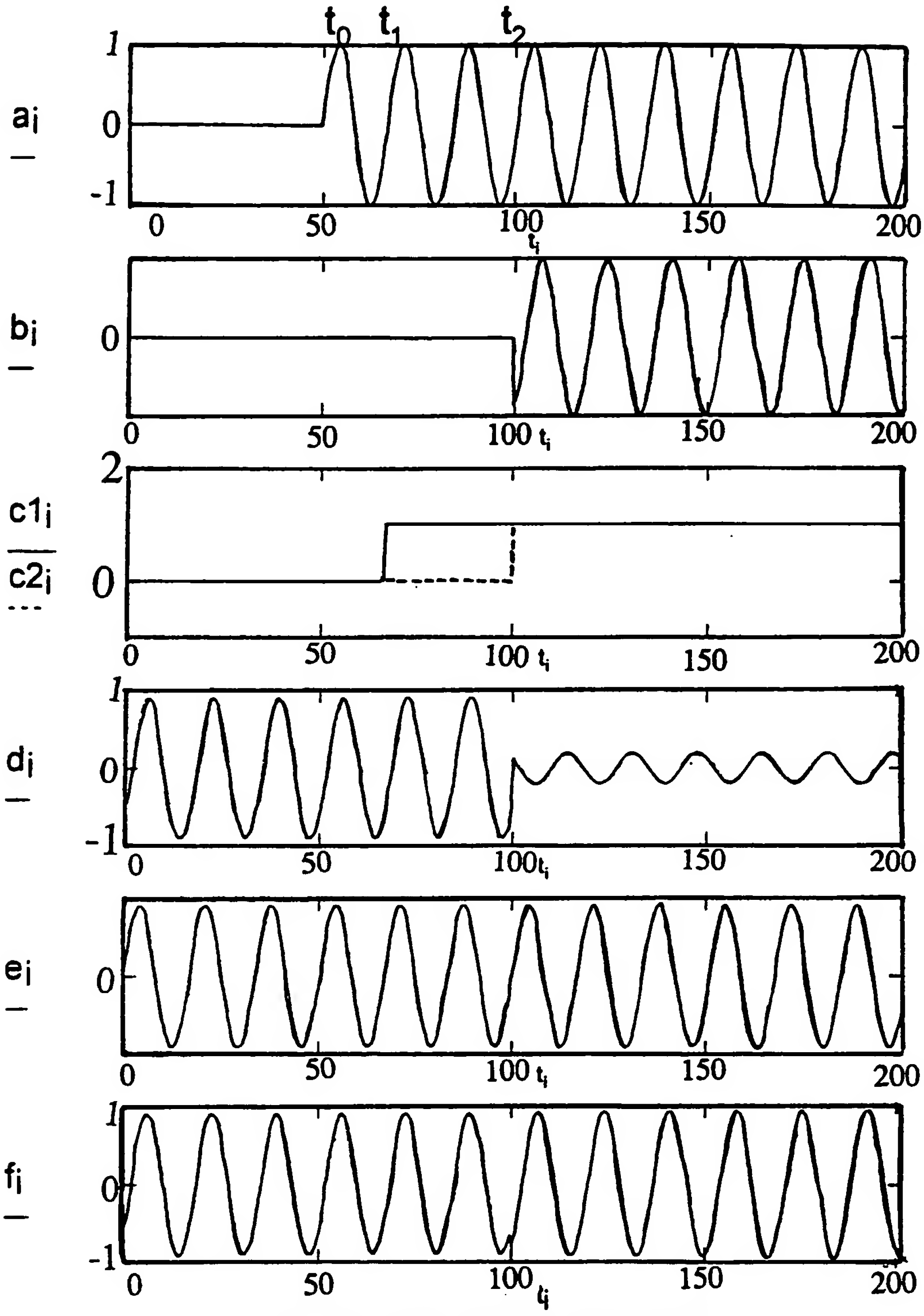
t0
t1
ai
bi
ci
di
ei
fi
1
0
-1
2
0
20
40
60
80
100
ti
X AXIS: TIME IN MILLISECONDS

FIGURE 27



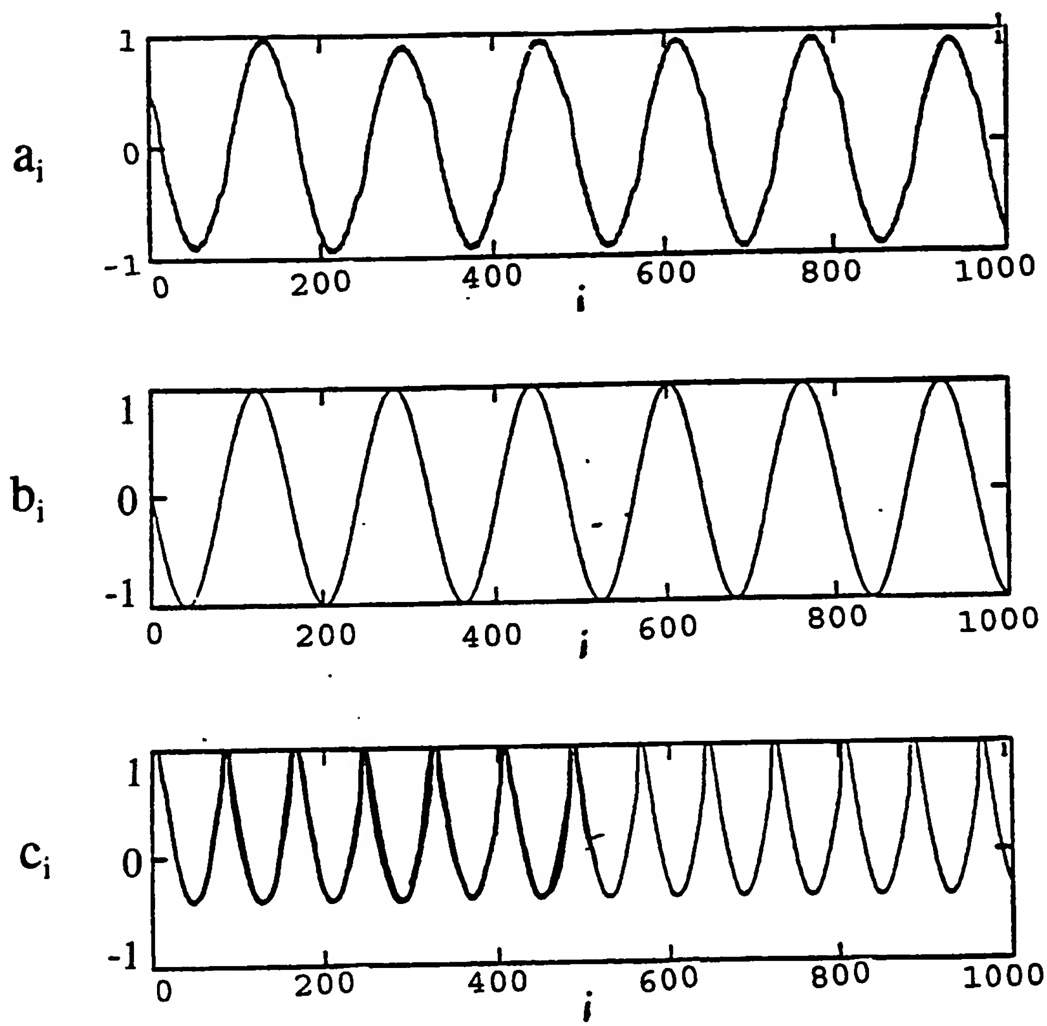
t0
t1
ai
bi
ci
di
ei
fi
1
0
-1
2
0
20
40
ti
60
80
100
X AXIS: TIME IN MILLISECONDS

FIGURE 28



X AXIS: TIME IN MILLISECONDS

FIGURE 29



a_i
1
0
-1
0
200
400
600
800
1000
i
b_i
1
0
-1
0
200
400
600
800
1000
i
c_i
1
0
-1
0
200
400
600
800
1000
i

Figure 30

2287843

Bimodal Fast Transfer Off-Line Uninterruptible Power Supply

The present invention relates to an uninterruptible power supply (UPS) which provides uninterrupted single-phase alternating current (AC) power supply to electrical loads using energy storage batteries as backup power elements. More particularly, the invention relates to an off-line UPS system where, when the AC mains is interrupted, the backup system connects to the load in a transient manner.

Interruptions in AC electrical power supply systems are common from either natural or man-made causes. Critical and/or sensitive electrical systems such as computerized electronic systems often require power without interruptions to operate. For such systems, an uninterruptible power supply (UPS) provides uninterrupted power during a mains power supply outage from backup systems such as energy storage batteries. In the case of a battery backup system, the batteries provide direct current (DC) power, thereby requiring DC power to AC power conversion with a nominal voltage and frequency identical to that of the mains AC power.

UPS systems can be broadly classified into two categories, namely, on-line and off-line. Typically, in an on-line UPS, the output AC power is generated by processing either the mains AC power when available, or the battery DC power when the mains AC power is not available. When the mains AC power is available, it is first converted to a DC bus power which in turn is converted to the output AC power. The batteries are interfaced either directly or indirectly to the DC bus. In the event of loss of the mains AC power, the batteries supply the DC bus power which in turn is converted to the output AC power.

Typically, in off-line UPS, the mains input AC power

when available is directly fed to the electrical load. In the event of the loss of the mains AC power, the battery DC power is converted to output AC power where the electrical load is transferred through a static transfer switch.

Generating AC output power by an on-line UPS through processing the DC bus power facilitates tailoring the AC output power to specific electrical load power quality requirements. As well, the interface of the battery to the DC bus allows the electrical load transfer between the mains and the backup system to be achieved without a transient break. The disadvantage of on-line UPS system is that the input AC to DC bus and the DC bus to output AC power conversions is less efficient than off-line UPS systems where there is no power conversion from the AC mains to the output.

In the past, off-line UPS systems achieved electrical load transfer between the AC mains and the backup system only in a transient manner by using a transfer switch. Such transients may be tolerable by most electrical loads if the transient profile is held within allowable limits and the recovery from the transient is made quickly.

In either on-line or off-line UPS systems, the batteries are charged using the mains AC power through a charging circuit. The charging power is typically only a fraction of the UPS power rating due to the short duration a conventional UPS is expected to provide backup power. In on-line UPS systems, the charging power is normally derived from the DC bus power.

In off-line UPS systems, the charging power is derived from the AC mains through a separate AC-DC converter. If the battery DC power to output AC power

conversion is achieved without galvanic isolation, it may be necessary to achieve the charger AC-DC conversion with such isolation. As the charging power is only a fraction of the UPS power rating, the cost of providing the isolation is only marginal. The battery charging mechanism, being based on AC-DC conversion, may introduce harmonic current components into the mains AC system. These harmonic currents, in large quantities, may be detrimental to the mains AC system components or intervene in the operation of other electrical loads connected to it. However, if the charging power is small, the corresponding harmonic currents are also small and limited within allowable limits by industry standards.

There has been a need to improve conversion efficiencies of power converters with the proliferation of critical and sensitive electrical loads such as computerized electronic systems which demand high power quality. It is, therefore beneficial to design off-line UPS systems which provide quality power akin to on-line UPS systems while maintaining high efficiency. This requires a network topology which allows a very fast electrical load transfer between the mains and the backup system supported by a very high speed monitoring and control of the mains and backup system signals.

Furthermore, the growing trend of many system requirements demanding the use of UPS systems with high power rating and extended backup time durations, it is imperative that such an off-line UPS system increases the capacity of its battery charging mechanism with little or no additional cost.

G. O. Sullivan (PCIM Magazine, December 1988 "Bimode UPS cuts system complexity, improves reliability) describes a network topology which utilizes an isolation transformer for interfacing the backup system with the AC

mains. Low frequency isolation transformers are, in general, bulky and heavy. To meet the objective of maximizing power conversion density for a given volume, size and weight limitations, it is desirable to eliminate the necessity of using low frequency isolation transformers.

In addition to the above objectives, it is imperative that the harmonic currents generated by the battery charging mechanism is limited to very small levels.

It is an object of the present invention to provide a single-phase off-line uninterruptible power supply system with a configuration in which a battery back-up circuit which operates in a bimodal manner, is interfaced with the output node of the UPS directly, without an isolation transformer, which system facilitates the transfer of the connected electrical load to/from the battery backup circuit from/to the AC mains in a very fast manner so as to minimize power outage to the load.

It is another object of the present invention to provide a UPS whereby, in the event of interruption or excursion into out-of-tolerance condition of the AC mains and in the event of its recovery to in-tolerance condition, the load can be transferred to and from, respectively, the backup circuit in a very fast and smooth manner, such that the disruption in single phase power being supplied to the load is minimized.

It is also an object of the present invention to regulate the UPS backup circuit output power with a feedback control system, based on a high speed DSP based

control system so that in the event of load transfer from the mains, the transients seen by the electrical load are minimum.

It is still another object of the invention to provide a UPS with a backup circuit functioning in a bimodal manner, to the most extent possible for both mains and backup modes in order to maximize their utilization and minimize the overall parts count of the UPS.

Another object of the invention is to shape the mains AC current waveform which provide the battery charging signal such that harmonic currents in the AC mains resulting due to battery charging are substantially reduced and the resultant AC fundamental current component has a very high power factor.

In accordance with the invention there is provided a single phase off-line uninterruptible power supply system for direct and continuous supply of an AC signal with in-tolerance voltage and in-tolerance frequency to an electrical load connected to an output node of said system, said system comprising: a transfer switch connected between an AC mains node and said output node, controlled for switching between a mains mode and a backup mode; a backup circuit connected between said output node and a backup battery node, for receiving the AC mains power supply signal and generating a battery charge signal on said battery node, while maintaining a high AC mains power factor, in said mains mode, and receiving a battery DC voltage on said battery node and converting it into said AC signal on said output node in said backup mode; an AC mains monitor unit which continuously senses said AC mains power supply signal for determining an out-of-tolerance condition and generating a mode transfer signal; a mode transfer control unit for

receiving said mode transfer signal and configuring and controlling said backup circuit in a battery charging configuration during said mains mode and in an inverter configuration during said backup mode, said battery charging and said inverter configurations sharing a number of electric components; and a control unit for controlling said transfer switch, said backup circuit, said AC mains monitor unit said mode transfer control unit.

The battery charging configuration of the UPS comprises: a single phase full bridge inverter, each arm of the bridge including an unidirectional high frequency switching element together with an anti-parallel diode, said inverter bridge for receiving and rectifying said AC mains power supply signal to a first DC signal on a first node, using a rectifier bridge formed by said anti-parallel diodes of said inverter bridge, while a second control signal disables said switching elements of said inverter bridge; a power factor corrector connected between said first node and a second node for receiving said first DC signal and generating a second DC signal of a higher voltage, for maintaining the harmonic current resulting at said AC mains node at a negligible level and for increasing the power factor of said AC signal, under the control of a third control signal; a battery charger connected between said second node and said battery node, for converting said second DC signal into said battery charge signal, under the control of a fourth control signal; and an inverter bridge filter connected between said inverter bridge and said output node for further correcting the power factor of said AC signal.

The inverter configuration of the UPS comprises: a battery voltage booster for receiving a battery voltage on said battery node and generating a third DC signal on a first node according to a fifth control signal; a

single phase full bridge inverter, each arm of the bridge including an unidirectional high frequency switching element together with an anti-parallel diode, for receiving said third DC signal on said first node and converting it into an inverted AC signal; an inverter bridge filter connected between said inverter bridge and said output node for filtering said inverted AC signal and delivering said AC signal to said output node; and a capacitor connected to said battery node for filtering the variations of said battery voltage.

The UPS further comprises a by-pass switch connected between said first and said second node for including said power factor corrector into said battery charging configuration, according to a sixth control signal.

According to another aspect of the present invention, there is provided a single phase off-line uninterruptible power supply system for direct and continuous supply of an AC signal with in-tolerance voltage and in-tolerance frequency to an electrical load connected to an output node of said system, said system comprising: a transfer switch connected between an AC mains node and said output node, controlled for switching between a mains mode and a backup mode; a single phase full bridge inverter, each arm of the bridge including an unidirectional high frequency switching element together with an anti-parallel diode, said inverter bridge for receiving and rectifying said AC mains power supply signal to provide a first DC signal on a first node, using a rectifier bridge formed by said anti-parallel diodes of said inverter bridge, while a second control signal disables said switching elements of said inverter bridge in said mains mode and for receiving a third DC signal on said first node and converting it into an inverted AC signal in said backup mode; a power factor corrector connected between said first node and a second

node, in said mains mode, for receiving said first DC signal and generating a second DC signal of a higher voltage, for maintaining the harmonic current resulting at said AC mains node at a negligible level and for increasing the power factor of said AC signal, under the control of a third control signal; a by-pass switch connected between said first and said second node for including said power factor corrector into said battery charging configuration and excluding the same from said inverter configuration, according to a sixth control signal; a battery charger connected between said second node and said battery node, for converting said second DC signal into said battery charging voltage, under the control of a fourth control signal, in said mains mode; an inverter bridge filter connected between said inverter bridge and said output node for further correcting the power factor of said AC mains power supply signal in said mains mode and for filtering said inverted AC signal and delivering said AC signal to said output node in said backup mode; a battery voltage booster for receiving a battery voltage on said battery node and generating a third DC signal on said first node according to a fifth control signal, in said backup mode; an AC mains monitor unit which continuously senses said AC mains power supply signal and determines an out-of-tolerance condition; a mode transfer control unit for receiving said mode transfer signal and generating control signals for configuring said backup circuit in a battery charging configuration during said mains mode and in an inverter configuration during said backup mode, said battery charging and said inverter configurations sharing a number of electric components; and a control unit for controlling said monitoring unit, said mode transfer unit, said transfer switch, said inverter, said power factor corrector, said by-pass switch, said battery charger, said inverter bridge filter and said battery voltage booster.

Advantageously, the UPS of the present invention provides uninterrupted single-phase alternating current supply in an improved manner by directly connecting the backup circuit without electrical isolation to the output node and hence facilitates a fast mechanism of the electrical load transfer between the mains and the battery supplies. The elimination of the necessity for an isolation transformer between the battery backup system and the AC mains facilitates the packaging of the UPS in a small volume with light weight.

Another advantage of the present system is that it allows the batteries of the backup system to be charged an discharged through a bimodal network which reduces the parts count and improves the system reliability.

Still another advantage is the presence of a mechanism to draw harmonic-free high power factor AC mains current for charging the batteries. The UPS is controlled by a microprocessor using high performance monitoring and control functions which aid in improving the output power quality.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other features of the invention will become more apparent from the following description in which reference is made to the appended drawings wherein:

FIGURE 1 is a simplified block diagram of the invention;

FIGURE 2a is a detailed functional block diagram of the invention;

FIGURE 2b illustrate an equivalent block diagram for the mains mode;

FIGURE 2c illustrate an equivalent block diagram for the back up mode;

FIGURE 3 shows the waveform of current through a resistive load with an AC voltage impressed across the resistor;

FIGURE 4 shows the waveform of the current through an AC voltage applied across the inductor;

FIGURE 5 shows the waveform of the current through a capacitive load on an AC voltage applied across the capacitor;

FIGURE 6 depicts a circuit configuration of the inverter bridge;

FIGURE 7 shows the generation of a PWM signal;

FIGURE 8 shows an illustration of the rectifier input and output voltage waveforms;

FIGURE 9 is a schematic diagram of the power factor corrector (PFC) circuit;

FIGURE 10 is the waveform of the PWM modulation signal for the power factor correction;

FIGURE 11 is a schematic diagram of the battery charger (BC) circuit;

FIGURE 12 is a schematic diagram of the battery voltage booster (BVB) circuit;

FIGURE 13 depicts the functional elements of the monitoring and control unit;

FIGURE 14 is a block diagram of the microprocessor of the monitoring and control unit;

FIGURE 15 is a flow diagram of the monitoring and control operation;

FIGURE 16 is a block diagram of the control scheme for the BVB;

FIGURE 17 is a block diagram of the control scheme for the inverter;

FIGURE 18 is a block diagram of the control scheme for the PFC;

FIGURE 19 is a block diagram of the control scheme for the battery charger;

FIGURE 20 illustrates the timing diagram for various control signals during transfer from the mains to the backup mode;

FIGURE 21 illustrates the timing diagram for various control signals during transfer from the backup to the mains mode;

FIGURE 22 depicts the power flow in the UPS in the mains mode;

FIGURE 23 depicts the power flow in the UPS in the backup mode;

FIGURE 24 illustrates the UPS transfer characteristic for a sudden loss of the AC mains power;

FIGURE 25 illustrates the UPS transfer characteristic for a sudden decrease in the AC mains voltage below the tolerance band;

FIGURE 26 illustrates the UPS transfer characteristic for a sudden increase in the AC mains voltage above the tolerance band;

FIGURE 27 illustrates the UPS transfer characteristic for a sudden decrease in the AC mains frequency below the tolerance band;

FIGURE 28 illustrates the UPS transfer characteristic for a sudden increase in the AC mains frequency above the tolerance band;

FIGURE 29 illustrates the UPS transfer characteristic for a transfer from the backup to the mains mode;

FIGURE 30 illustrates the AC mains current supplying the

battery charging power.

The bimodal fast transfer UPS (BMFTUPS) implements a new scheme of interfacing AC mains power and a battery backup system as shown in Figure 1. The BMFTUPS 10 is shown having a transfer switch 12 connecting an AC mains power source 14 and load 16. A battery backup system 18 is connected to an output node 20 via a booster/charger 22 and inverter/rectifier 24.

The AC mains 14 is typically 115 V (+/-10%), 60 Hz (+/-5%) single-phase AC which may be subjected to momentary or prolonged interruption. The input voltage and/or frequency of the AC mains 14 may also make excursions above or below the tolerance band acceptable by the connected electrical load 16 for a sustained period as described below.

The batteries 18 for supplying the backup power are rechargeable (secondary) cells, for example sealed lead acid gel-cel. The batteries 18 are connected in a series and/or parallel configuration, with a series configuration providing the basic terminal voltage level and a parallel configuration providing increased discharge current capacity. Typically, twelve batteries each with a nominal terminal voltage of 12 VDC are connected in series to obtain a nominal battery bank terminal voltage of 144 VDC. A single circuit with each battery rated at 15 ampere-hours (AH) is used to provide 2 KW UPS output power for 25 minute backup duration. The backup power duration of the UPS can be increased within reasonable limits by adding in parallel a number of series connected batteries.

The intended electrical load 16 is connected to

the output node 20 of the UPS. Typically, the load 16 requires uninterrupted power and cannot tolerate voltage level outside 115 V +/-5% for more than half a cycle of the power frequency cycle or a steady-state frequency outside 60 Hz +/-5%. As well, the load 16 may have capacitive or inductive elements, causing a leading or lagging power factor up to 0.8. The power factor is defined as the cosine of the angle between the voltage across the load and its associated current therethrough. As shown in Figure 3, for a purely resistive load the current waveform (iR in Figure 3) is in phase with the voltage and the power factor equals 1.0. For a purely inductive load, the current lags the voltage by 90 degrees and for a purely capacitive load the current leads the voltage by 90 degrees. Figures 4 and 5 show the practical waveform of the voltage and current in the case of an inductive (Figure 3, iL), respectively capacitive (Figure 4, iC) load.

A detailed functional block and circuit diagram of the BMFTUPS 10 is shown in Figure 2 comprising the following components:

1. TRANSFER SWITCH 12- The transfer switch 12 comprises a pair of unidirectional static switching elements 26 connected back-to-back. Each switching element can be made to conduct current in only one direction as indicated by the arrows (Figures 1 and 2) by providing a gate control signal if the switch is forward biased in the direction of current conduction. Thus, the back-to-back connected switching elements when turned on provide current path in both directions. The transfer switch 12 can be any type of switching device, which can be turned on or off by a gating control signal.

2. INVERTER 28 - The inverter 28 is shown in Figs. 2 and 6. It performs the function of DC-AC conversion in the

backup mode and the function of an AC-DC rectifier in the mains mode. The output of inverter bridge 28 is filtered by an inverter filter 30 which the DC output is processed for obtaining the charging current for battery 18.

IN THE BACKUP MODE - The inverter bridge 28 is a single phase full bridge network as shown in Figure 6 consisting of unidirectional high frequency switching elements 32 (Q1, Q2, Q3 and Q4) together with anti-parallel diodes 34 (D1, D2, D3 and D4) in each arm of the bridge 28. The configuration of the backup circuit in the backup mode is shown in Figure 2c. The bridge 28 is supplied at input node 1-1′ with the DC output voltage V3 of the battery voltage booster 36 to be described later, collected on node 3-3′. The switching elements Q1 through Q4 of the bridge network are turned on and off using a set of high frequency PWM (pulse width modulation) signals shown in Figure 7 each modulated with a periodic reference sinusoidal waveform 100 with the nominal frequency of the AC mains. Each PWM signal toggles between a logic high level and a logic low level. Signal PWM(+) is generated by comparing the sinusoidal modulating wave SIN(+) with a triangular carrier wave 102. At the instants when the modulating wave is higher than the carrier wave, PWM(+) signal is set high, otherwise it is set low. Signal PWM(-) is generated in a similar manner by comparing the waveform SIN(-) (which is the inverse of the waveform SIN(+)) with the carrier triangular wave. The application of PWM(+) and PWM(-) signals to the gates of the bridge switching element pairs Q1, Q4 and Q2, Q3 respectively, results in the impression of the boost chopper DC voltage across the bridge output 2-2′ with alternating positive and negative polarity. Thus, the output of the bridge network is an AC periodic sinusoidal power with the nominal frequency of the AC mains riding on a carrier waveform with the frequency of the PWM signal. Typically, the AC mains frequency is 60 Hz and the PWM frequency is

19,200 Hz. The amplitude, frequency and the precision of the sinusoidal output power is directly related to the amplitude, frequency and precision, respectively, of the reference sinusoidal waveform and hence can be altered by modifying the reference sinusoidal waveform. The inverter bridge 28 can supply a resistive, inductive or capacitive load and hence the bridge output current can be in phase with, lag or lead the bridge output voltage. The anti-parallel diodes D1 to D4 of the bridge 28 provide a path for the commutating current whenever the bridge current is either lagging or leading the bridge output voltage and interrupted by the opening of a switching element and the closing of any other switching element at the same instant does not provide a current path.

IN THE MAINS MODE - The configuration of the backup circuit in the mains mode is shown in Figure 2b. The rectifier 40 is operational only during the mains mode and converts the AC mains voltage to an unregulated DC voltage for supplying battery charging power. It is connected to the output node 20 of the UPS through terminals 2-2′. It is made up of the single-phase full bridge network formed by the anti-parallel diodes D1 through D4 of the inverter bridge 28 shown in Figure 6. The rectifier output collected on terminals 1-1′ is full-wave rectified sinewave as shown in Figure 8. The AC-DC power conversion through this rectifier is possible only with the switching elements Q1 through Q4 of the inverter bridge 28 turned off.

3. INVERTER FILTER 30 - The inverter filter 30 is an inductive-capacitive (LC) circuit connected as shown in Figures 2 and 6 and filters the high frequency PWM carrier waveform present in the inverter bridge output to obtain AC sinusoidal power with the nominal frequency of the mains AC power. The inductors 104 and the capacitor 106 are chosen so as to limit the inverter output voltage

harmonic components related to the switching frequency of the inverter bridge 28 below a tolerable level. The inductors 104 of the inverter filter provide additional line inductance to the power factor corrector 38 when the UPS is operating in the mains mode and hence performs bimodally as filter or as additional power factor corrector.

4. POWER FACTOR CORRECTOR 38 - In the mains mode, while charging the batteries 18, the UPS backup system circuit provides that the waveform of the AC current drawn from the AC mains 14 is near sinusoidal and closely in phase with the mains AC voltage waveform. Thus, it ensures that the harmonic currents resulting in the mains due to battery charging are negligibly small and that the mains AC current has a high power factor. This is accomplished by a boost DC-DC converter based power factor correction (PFC) network 38, shown in Figures 2b and 9, connected between the rectifier 40 terminals 1-1′ and terminals 3-3′ of the charging circuit 44. The switching element Q5 of the PFC is turned on and off using a high frequency pulse-width-modulation (PWM) signal with a reference periodic waveform as the modulation signal. The high frequency carrier waveform in the resulting output voltage is filtered using a DC capacitor C7. The inductive energy in the inductor L5 of the PFC is charged by the rectifier output voltage through the switching element Q5 when Q5 is turned on and discharges into the PFC load at terminals 3-3′ when Q5 is turned off. Diode D5 prevents a power flow from the PFC 38 output through Q5 and ensures that the PFC output voltage is always greater than or equal to its input voltage. Thus, a power transfer is achieved in the direction from the rectifier to the PFC output with a voltage gain greater than unity. The waveform of the current through L5 is shaped to a rectified sinusoidal waveform riding on the PWM carrier by choosing the modulation waveform as shown in Figure

10. S. Sivakumar, K. Natarajan, "Kalman filter based high speed measurement and control of AC voltages for UPS applications", 1993 IEEE Power Electronics Specialists Conference Record, Seattle, Washington, June 1993. This modulation signal has a "sliced" rectified sinusoidal waveform with a phase shift ϕ measured from the AC mains voltage waveform and a per unit amplitude α. In a broad sense, PFC voltage gain can be increased by increasing α and the AC mains current power factor for increased battery charging current can be maximized by increasing ϕ. Hence, by using a feedback signal based on sensed battery charging voltage and current, both α and ϕ can be adjusted to obtain regulated PFC output voltage with a high AC mains current power factor. Typically, the PFC output voltage is regulated at a 200 VDC and the AC mains current power factor is maintained above 0.9 for the full range of battery charging currents for 15 AH batteries with a maximum of 10 A.

5. BATTERY CHARGER 44- In the mains mode, as shown in Figure 2b the precise charging of the batteries of the backup system is achieved using a battery charger 44 which is a buck DC-DC converter which converts the PFC output DC voltage V2 at terminals 3-3′ to a regulated and current limited battery charging DC voltage Vbc on terminals 5-5′. The switching element of the buck converter is turned on and off using a high frequency PWM signal with a feedback signal derived from the battery charging voltage and current signals as the modulation signal. The battery charger 44 is shown in Figure 11. When the switching element Q6 is turned on, the inductive energy in the inductor L6 is charged by the PFC output voltage through the load at terminals 5-5′, namely battery 18. When Q6 is turned off, inductive energy is discharged into the battery through the diode D6. Capacitor C6 filters the high frequency PWM carrier so as to obtain a smooth DC output voltage. Thus, a power flow

in the direction from the PFC output to the buck converter output is achieved with a voltage gain of less than unity. Typically, the PFC output voltage of 200 VDC is converted to a regulated 165 VDC battery charging voltage to charge 12 batteries 18 of nominal terminal voltage of 12 VDC each connected in series. The battery charging voltage and current are directly related to, and can be altered by varying, the modulation signal. The high frequency carrier waveform in the resulting output voltage is filtered using an inductor-capacitor (LC) filter.

6. BATTERY VOLTAGE BOOSTER 36 - In the backup mode, illustrated in Figure 2c, the battery DC voltage needs to be boosted up to a specific voltage level prior to feeding to the inverter 28 in order to obtain the nominal output AC voltage level. This is accomplished using a battery voltage booster 36 (BVB) which is a boost DC-DC converter which converts the unregulated battery DC voltage input Vb at terminals 5-5′ to a regulated DC voltage V3 at inverter input 1-1′. The battery voltage booster 36 is shown in Figure 12. The inductive energy in the inductor L7 of the boost converter is charged by the battery voltage Vb through the switching element Q7 when Q7 is turned on and discharges into the load at terminals 3-3′ when Q7 is turned off. Diode D7 prevents a power flow from the BVB output 3-3′ through Q3 and ensures that the BVB gain is always greater than or equal to unity. Thus a power transfer is achieved in the direction from the batteries 18 to the BVB output. Typically, the BVB 36 converts the 144 VDC nominal battery bank voltage at terminals 5-5′ to a regulated 250 VDC output voltage at terminals 3-3′. The battery 18 terminal voltag vary between 163 VDC (when fully charged) to 1 (when almost fully discharged). The switching of the boost converter is turned on and off usi frequency PWM signal with a feedback signal der

the BVB output DC voltage V3 as the modulation signal. The output voltage regulation of the boost converter is directly related to, and hence can be modified by varying, the modulation signal.

7. PFC BYPASS SWITCH (48) - The power factor corrector 38 needs to be bypassed when the UPS is operating in the backup mode. This is accomplished by the PFC bypass switch (PFCBS) which is a unidirectional switch which is connected between terminals 1 and 3 (Figs. 2a, 2b, 2c). When turned on, by-pass switch 48 connects the BVB 36 output 3 directly to the inverter 28 input allowing a power flow from the BVB 36 to the inverter. The bypass switch 48 is turned off in the mains mode which activates the PFC 38.

8. MONITORING AND CONTROL - The monitoring and control functions are provided by a monitoring and control unit 50 (e.g. a microprocessor). The functions of unit 50 are grouped into four categories as shown in Figure 13: AC mains monitoring 52, BVB and inverter control 54, battery charging control 56 and mode transfer control 58.

The flow diagram of the monitor and control operation is shown in Figure 14. The MCU 50 includes a CPU chip 60 such as a National Semiconductor HP 16003 sixteen-bit processor connected by means of a common bus to read only memory (ROM) 62 and an input/ output (I/O) unit 64 which enables the communication between the MCU 50 and the various elements shown in Figure 2. The functions of the AC mains monitoring, inverter control, battery charging control and mode transfer control are embodied as encoded instructions which are stored either in the ROM 62 and are executed as appropriate by the CPU 60, to enable it to send command signals through the I/O to the rest of the elements in the system of Figure 2. The signals input to and output from the I/O unit are

typically digital signals which are converted by analog-to digital, digital-to analog and digital-to-PWM converters for appropriate interfacing with various system components in Figure 2.

The AC mains monitoring unit mode of operation will be explained further, reference being also made to Figure 15. The in- or out-of-specification condition of the AC mains, voltage and frequency are determined by the microprocessor using a Kalman filter based DSP model. S. Sivakumar, K. Natarajan, "Single phase power factor correction with sliced sinewave PWM modulation", Joint Technical Report, K.B. Electronics (1989) Ltd. and Lakehead University, Report No. KBE92-027, June 1992. In this, the mains AC voltage waveform is continuously sensed and compared with a reference waveform modelled internally in the microprocessor 50. The frequency of the model waveform is set at the nominal AC mains power frequency, typically 60 Hz. The error between the sensed and the modelled waveforms is used in an iterative manner in order to force the Kalman filter output to track the sensed AC mains waveform. When the AC mains power frequency exactly matches the model waveform frequency, after few initial iterative cycles, the Kalman filter output tracks the sensed AC mains waveform, with zero steady-state error. In this process, the Kalman filter generates a set of state-variable estimates which provide information on the voltage magnitude and the frequency of the sensed AC mains waveform. By appropriately combining these state variables, the microprocessor 50 determines the root-mean-square (rms) value of the AC mains voltage (steps S28-S6) and its frequency deviation from the nominal frequency (steps S7). As this estimation process is based on a predictive approach using an internal model waveform, the variations in the rms voltage and the frequency of the AC mains, and hence their in- or out-of-specification condition are "instantaneously" determined

at each iteration. In choosing the Kalman filter parameters, the speed of response and the degree of noise rejection are traded-off with each other to guarantee optimal performance of the filter. When the estimated rms voltage and the frequency falls outside the range of acceptable tolerance bands, the microprocessor initiates appropriate control action to operate the UPS in backup mode. Typically, the voltage tolerance band is chosen as 115 VAC +/-5% and the frequency tolerance band is chosen as 60 Hz +/-3%.

The control unit comprises circuits for controlling the units of the backup circuit in both the mains and backup modes.

The configuration of the BVB control scheme is shown in Figure 16. When the UPS operates in the backup mode, the PWM control signal for Q7 of the battery voltage booster (BVB) 36 is generated by the microprocessor 50 using the voltage and current of the BVB output signal V3 as the feedback signals. The voltage sensed on terminal 3 is compared with a preset reference voltage in comparator 70 to generate an error signal which in turn is processed through a PI control loop 68 to generate the modulation signal for the PWM generator 72. The PWM signal is generated by comparing the modulation signal with a triangular carrier wave similar to the case illustrated in Figure 7. This enables the BVB output voltage to be regulated at the reference voltage level when the sensed BVB output current is sensed by current sensor 74 and compared with a current limit set in block 76. When it exceeds a preset safety limit, the reference voltage is appropriately reduced in comparator 78 (see step S3) so that the BVB output voltage is regulated at a lower level which reduces the BVB output current below the safety limit.

The inverter control signal is generated by sensing the inverter output voltage and using a Kalman filter based DSP model similar to that used for the AC mains monitoring discussed above. The configuration of the inverter control scheme is shown in Figure 17. The inverted AC voltage on output 2 is continuously sensed and compared with a reference waveform modelled internally in the microprocessor 50 through a Kalman filter 80. The frequency of the model waveform detected in comparator 82 is set at the nominal inverter power frequency, typically 60 Hz. The error between the sensed and the modelled waveforms is used in an iterative manner in order to force the Kalman filter output to track the sensed inverter output waveform. After a few initial iteration cycles, the Kalman filter output perfectly tracks the sensed inverter waveform, with zero steady-state error. In this process, the Kalman filter generates a set of state-variable estimates which provide information on the voltage magnitude of the sensed inverter output waveform. By appropriately combining these state variables, the microprocessor 50 determines the rms value of the inverter output voltage in estimator 84. This estimated rms value is compared in comparator 86 with a reference value for the inverter to generate an error signal, which in turn is processed in a proportional-integral (PI) type feedback control loop 88 to generate the inverter control signal. This signal, in turn, instantaneously modifies the amplitude of a sinusoidal reference generator 90. The amplitude modulator 92 modulates the PWM signals of generator 94 which in turn control the gating of the inverter switching elements. This enables a precise regulation of the inverter output voltage. The PWM signal is generated by comparing the modulation signal with a triangular carrier wave as shown in Figure 7. The gain parameters of the PI controller 88 are chosen appropriately to ensure the transient response of the inverter output voltage for

load and input voltage changes are kept minimal with a fast recovery to steady-state.

The configuration of the PFC control scheme is shown in Figure 18. The PWM control signal for switch Q5 of the power factor corrector (PFC) is generated by the microprocessor 50 by using the state-variable estimates obtained in the process of AC mains monitoring described above. The state-variable estimates are suitably weighted and combined in sliced rectified sinewave generator 96 to obtain the sliced rectified sinusoidal waveform. This waveform is used as the modulation signal of a PWM waveform 98 which controls the gating of the PFC switching element Q5. The PWM signal is generated by comparing the modulation signal with a triangular carrier wave similar to the case illustrated in Figure 7. The phase shift ϕ and the per-unit amplitude α of this modulation signal, and hence the regulation of the PFC output voltage and the AC mains current power factor, can be varied by suitably modifying the state-variable weighting factors in phase-shift and amplitude control unit 110. The weighting factors are determined using a feedback signal based on the battery charging voltage and current sensed in current sense unit 112 in order to achieve desired PFC output voltage regulation with a high AC mains current power factor.

The configuration of the battery charger control scheme is shown in Figure 19. The PWM control signal for the battery charger is generated using the sensed battery voltage and charging current as the feedback signals. The sensed battery voltage is compared with a preset reference voltage in comparator 114 to generate an error signal which in turn is processed through a PI control loop 116 to generate the modulation signal for the PWM signal. The PWM signal is generated in PWM generator 118 by comparing the modulation signal with a triangular

carrier wave similar to the case illustrated in Figure 7. This effects the regulation of the battery charging voltage at the reference voltage level. When the sensed battery charging current exceeds a preset limit, this is detected by current sensor unit 120. The reference voltage is appropriately reduced in comparator 122 so that the battery charging voltage is regulated at a lower level which reduces the charging current below the limit.

The mode transfer control unit operates as described in the following. The timing diagram of the control signals for the mode transfer from the mains to the backup is shown in Figure 20 with reference to Figs. 2B and 2C. The UPS operating mode transfer between the mains and the backup is effected by the microprocessor 50 by sending appropriate on/off control signals to the various elements of Figure 2A. When the UPS is operating in the mains mode, at the instant of detection of an out-of-specification condition by the AC mains monitoring function at instant t_0 as shown in trace (a), the microprocessor 50 generates a disable command signal at instant t_1 to the transfer switch 12, the battery charger 44 and the power factor corrector 38 simultaneously as shown in trace (b). These elements turn-off at instant t_2 with a time lag as shown in trace (c) due to the time spent for the transmission of the turn-off command signal. The microprocessor 50 generates and sends an enable command signal to the inverter 28, the battery voltage booster 36 and the PFC bypass switch 48 simultaneously at instant t_3 after a time-delay as shown in trace (d). This time-delay is required to ensure that the transfer switch 12, the battery charger 44 and the PFC 38 are completely turned off prior to the inverter 28, the BVB 36 and the PFC bypass switch 48 are turning on in order to avoid short circuits. The inverter 28, the BVB 36 and the PFC bypass switch 48 turn on at instant t_4 with a time lag as shown in trace (e) due to the time

spent for the transmission of the turn-on command signal.

The timing diagram of the control signals for the mode transfer from the backup to the mains is shown in Figure 21. When the UPS is operating in the backup mode and when the AC mains recovers to in-specification condition at instant t_0 as shown in trace (a), the microprocessor 50 starts monitoring the synchronism of the AC mains waveform and the inverter output waveform. After instant t_1 when the AC mains waveform gets to a close synchronism with the inverter output waveform as shown in trace (b), the microprocessor 50 generates and sends a disable command signal to the inverter, the BVB 36 and the PFC bypass switch 48 simultaneously at instant t_2 as shown in trace (c). These elements turn off at instant t_3 with a time lag due to the transmission delay of the off command signal. The microprocessor 50 generates and sends an enable command signal to the transfer switch 48, the PFC 38 and the battery charger simultaneously with a time-delay at instant t_4 shown in trace (e). This time-delay is required to ensure that the inverter 28, the BVB 36 and the PFC bypass switch 48 are completely turned off prior to the turn-on of the transfer switch 12, the PFC 38 and the battery charger 44 in order to avoid short circuits. The transfer switch 12, the PFC 38 and the battery charger 44 turn on at instant t_5 with a time lag as shown in trace (f) due to the transmission delay of the turn-on command signal.

The direction of power flow in the UPS 10 when it operates in the mains mode is shown in Figure 22. The transfer switch 12, the PFC 38 and the battery charger are enabled and the inverter 28, the BVB 36 and the PFC 38 are disabled. The AC mains supplies power to the electrical load through the transfer switch 12. It also supplies battery charging power through the rectifier 40, the PFC 38 and the battery charger 44 (see also Fig. 2B).

The direction of power flow in the UPS when it operates in the backup mode is shown in Figure 23. The BVB 36 and the inverter 28 are enabled and the transfer switch 12, the rectifier and the battery charger are disabled. The battery supplies power to the electrical load through the BVB 36 and the inverter 28.

EXAMPLES

Example 1

The operating characteristics of the UPS 10 during mode transfers from the mains to the backup for various cases of AC mains transition from the in-specification to the out-of-specification condition are illustrated in Figs. 24 through 29.

In Figure 24, the transfer characteristic of the UPS 10 for a sudden loss of the AC mains voltage is depicted. Prior to time instant t_0, the UPS 10 has been operating in the mains mode supplying an inductive load at 0.8 power factor. The AC mains voltage and current waveforms are shown in traces (a) and (b), respectively. In this period, although the inverter 28 is disabled, the generation of its sinusoidal reference waveform is enabled and synchronized to the AC mains voltage waveform. At instant t_0, the AC mains voltage suddenly drops to zero as shown in trace (a). The AC mains monitoring senses this drop as shown in trace (c) and the mode transfer control initiates a command to disable the transfer switch 12, the PFC 38 and the battery charger 44. The mode transfer control 58 initiates a second command to enable the inverter 28, BVB 36 and the PFCBS 48 which eventually turn on after a short time-delay not apparent in Figure 24. The inverter output current (filtered) and voltage waveforms are shown in traces (d) and (e) respectively. The current waveform in trace (d) prior to instant t_0 is that component of the AC mains

which supplies the battery charging power. The voltage waveform at the UPS output 20 as seen by the load is same as that of the voltage at the inverter output shown in trace (e). The current waveform at the UPS output as seen by the load is shown in trace (f). These waveforms are almost continuous with only small transient breaks which are limited to a very small time interval. Typically, also in these waveforms, the sinusoidal waveshape is preserved at the transition, evidently due to the synchronization of the inverter output voltage to the AC mains voltage.

Example 2

In Figure 25, the transfer characteristic of the UPS for a sudden reduction of the AC mains voltage below the 5% tolerance limit is shown. Prior to time instant t_0, the UPS 10 has been operating in the mains mode as in the case of Figure 24. At instant t_0, the AC mains voltage instantly drops below the 5% tolerance limit as shown in trace (a). Shown in trace (b) is the AC mains current waveform. The AC mains monitoring senses the voltage drop at instant t_1 as shown in trace (c) and the mode transfer control sends disable commands to the transfer switch 12, the PFC 38 and the battery charger 44 and enable commands to the inverter 28, the BVB 36 and the PFCBS 48 as described for the case of Fig. 24. The resulting filtered inverter current is shown in trace (d). The UPS 10 output voltage output current waveforms are shown in traces (e) and (f) respectively. These waveforms are almost continuous with virtually no transient breaks. The transfer time (duration between instants t_0 and t_1) is generally higher than the transfer time for the case of Figure 24 and is typically, 8.33 ms, equivalent to half a power frequency cycle.

Example 3

In Figure 26, the transfer characteristic of the UPS for a sudden increase of the AC mains voltage above the 5% tolerance limit is depicted. The UPS operates with a similar characteristic as that for the case of Figure 25.

Example 4

In Figure 27, the transfer characteristic of the UPS for a sudden reduction of the AC mains frequency below a 3% tolerance limit is shown. Prior to time instant t_0, the UPS has been operating in the mains mode as in the case of Figure 24. At instant t_0, the AC mains frequency drops below a 3% tolerance limit as shown in trace (a). The AC mains current waveform is shown in trace (b). The AC mains monitoring senses this drop at instant t_1 as shown in trace (c) and the mode transfer control sends disable and enable commands as described for the case of Figure 24. The resulting filtered inverter current is shown in trace (d). The resulting UPS output voltage and current waveforms are shown in traces (e) and (f) respectively. The transfer time (duration between instants t_0 and t_1) is generally higher than the transfer times for the cases of Figures 24 through 26 and is typically 16.67 ms, equivalent to a power frequency cycle.

Example 5

In Figure 28, the transfer characteristic of the UPS for a sudden increase of the AC mains frequency above a 3% tolerance limit is shown. The UPS operates with a similar characteristic as that for the case of Figure 27.

Example 6

In Figure 29, the transfer characteristic of the UPS for a transfer from the backup to the mains is shown. Prior to time instant t_0, the UPS has been operating in

the backup mode supplying an inductive load at 0.8 power factor. The AC mains current waveform is shown in trace (b). The inverter filtered current and voltage and waveforms are shown in traces (d) and (e) respectively. At instant t_0, the AC mains voltage recovers instantly from zero to its nominal value with its nominal frequency as shown in trace (a). The AC mains monitoring senses this recovery at instant t_1 as shown in trace (c). At this instant, the AC mains voltage and the inverter output voltage are not in synchronism as seen in traces (e) and (a). These waveforms eventually come to a close synchronism at instant t_2. In order to speed up the occurrence of this instant, the BVB and inverter control function of the microprocessor slowly varies the inverter output frequency on-line within the allowable tolerance limits. At instant t_2, the mode transfer control 58 initiates a command to disable the inverter 28, the BVB 36 and the PFCBS 48. The mode transfer control 58 also initiates a second command to enable the transfer switch 12, the PFC 38 and the battery charger 44 which eventually turn on after a short time-delay which is not apparent in Figure 29. The resulting voltage and current waveforms at the UPS output as seen by the load are shown in traces (e) and (f). These waveforms are almost continuous with virtually no transient breaks and preserve the sinusoidal waveshape at the transition.

The backup to the mains transfer characteristics of the UPS for the cases of the AC mains recovery from other out-of-specification conditions are similar to the case of Figure 29.

Example 7

In Figure 30, the battery charging characteristics of the UPS is shown. With the UPS operating in the mains mode with no connected electrical load, the steady-state

waveform of the AC mains current supplying the battery charging power through the rectifier 40, PFC 38 and the battery charger 44 is shown in trace (a). The AC mains voltage waveform is shown in trace (b). The modulation waveform of the PWM signal controlling the PFC is shown in trace (c). The shape of the AC mains current in nearly sinusoidal and is closely in phase with the AC mains voltage and hence has a high power factor.

Although a specific embodiment of the invention has been disclosed it would be understood by those having skill in the field of the invention that the minor changes can be made to the specific embodiment without departing from the spirit and the scope of the invention.

CLAIMS

1. A single phase off-line uninterruptible power supply system for direct and continuous supply of an AC signal with in-tolerance voltage and in-tolerance frequency to an electrical load connected to an output node of said system, said system comprising:

a transfer switch connected between an AC mains node and said output node, controlled for switching between a mains mode and a backup mode;

a backup circuit connected between said output node and a backup battery node, for receiving the AC mains power supply signal and generating a battery charge signal on said battery node in said mains mode, and receiving a battery DC voltage on said battery node and converting it into said AC signal on said output node in said backup mode;

an AC mains monitor unit which continuously senses said AC mains power supply signal for determining an out-of-tolerance condition and generating a mode transfer signal;

a mode transfer control unit for receiving said mode transfer signal and configuring said backup circuit in a battery charging configuration during said mains mode and in an inverter configuration during said backup mode, said battery charging and said inverter configurations sharing a number of electric components; and

a control unit for controlling said transfer switch, said back-up circuit, said AC mains monitor unit and said mode transfer control unit.

2. A system as claimed in claim 1, wherein said battery charging configuration comprises:

a single phase full bridge inverter, each arm of the bridge including an unidirectional high frequency switching element together with an anti-parallel diode,

said inverter bridge for receiving and rectifying said AC mains power supply signal to a first DC signal on a first node, using a rectifier bridge formed by said anti-parallel diodes of said inverter bridge, while a second control signal disables said switching elements of said inverter bridge;

a power factor corrector connected between said first node and a second node for receiving said first DC signal and generating a second DC signal of a higher voltage, for maintaining the harmonic current resulting at said AC mains node at a negligible level and for increasing the power factor of said AC signal, under the control of a third control signal;

a battery charger connected between said second node and said battery node, for converting said second DC signal into said battery charge signal, under the control of a fourth control signal; and

an inverter bridge filter connected between said inverter bridge and said output node for further correcting the power factor of said AC signal.

3. A system as claimed in claim 1, wherein said inverter configuration comprises:

a battery voltage booster for receiving a battery voltage on said battery node and generating a third DC signal on a second node according to a fifth control signal;

a single phase full bridge inverter, each arm of the bridge including an unidirectional high frequency switching element together with an anti-parallel diode, for receiving said third DC signal on said first node and converting it into an inverted AC signal;

an inverter bridge filter connected between said inverter bridge and said output node for filtering said inverted AC signal and delivering said AC signal to said output node;

a capacitor connected to said battery node for

filtering the variations of said battery voltage; and

a by-pass switch connected between said first and said second node for excluding said power factor corrector from said backup mode according to a sixth control signal

4. A system as claimed in claim 2, further comprising a by-pass switch connected between said first and said second node for including said power factor corrector into said battery charging configuration, according to a sixth control signal.

5. A single phase off-line uninterruptible power supply system for direct and continuous supply of an AC signal of with in-tolerance voltage and in-tolerance frequency to an electrical load connected to an output node of said system, said system comprising:

a transfer switch connected between an AC mains node and said output node, controlled for switching between a mains mode and a backup mode;

a single phase full bridge inverter, each arm of the bridge including an unidirectional high frequency switching element together with an anti-parallel diode, said inverter bridge for receiving and rectifying said AC mains power supply signal to provide a first DC signal on a first node, using a rectifier bridge formed by said anti-parallel diodes of said inverter bridge, while a second control signal disables said switching elements of said inverter bridge in said mains mode and for receiving a third DC signal on said first node and converting it into an inverted AC signal in said backup mode;

a power factor corrector connected between said first node and a second node, in said mains mode, for receiving said first DC signal and generating a second DC signal of a higher voltage, for maintaining the harmonic current resulting at said AC mains node at a negligible level and for increasing the power factor of said AC

signal, under the control of a third control signal;

a by-pass switch connected between said first and said second node for including said power factor corrector into said battery charging configuration and excluding the same from said inverter configuration, according to said sixth control signal;

a battery charger connected between said second node and said battery node, for converting said second DC signal into said battery charging voltage, under the control of a fourth control signal, in said mains mode;

an inverter bridge filter connected between said inverter bridge and said output node for further correcting the power factor of said AC mains power supply signal in said mains mode and for filtering said inverted AC signal and delivering said AC signal to said output node in said backup mode;

a battery voltage booster for receiving a battery voltage on said battery node and generating a third DC signal on said second node according to a fifth control signal, in said backup mode;

an AC mains monitor unit which continuously senses said AC mains power supply signal for determining an out -of-tolerance condition;

a mode transfer control unit for receiving a mode transfer signal and generating control signals for configuring said backup circuit in a battery charging configuration during said mains mode and in an inverter configuration during said backup mode, said battery charging and said inverter configurations sharing a number of electric components; and

a control unit for controlling said monitoring unit, said mode transfer unit, said transfer switch, said inverter, said power factor corrector, said by-pass switch, said battery charger, said inverter bridge filter and said battery voltage booster.

6. A system as claimed in claim 1 or 5, wherein said AC

mains monitoring unit comprises:

means for determining the mode of operation of the system;

means for continuously sensing said AC mains power supply signal;

means for generating a reference sinewave with a frequency equal with a target nominal frequency;

means for comparing said sensed AC mains supply voltage and said reference sinewave to obtain a difference signal;

Kalman filter means for receiving said difference signal and generating an output which traces said sensed AC mains power supply signal;

means for determining state variables for the estimated voltage and frequency of said output and for determining the root-mean-square value of voltage and frequency deviations;

means for generating said mode transfer signal if the estimated root-mean-square value of voltage or frequency falls outside a preset in-tolerance band.

7. A system as claimed in claim 1 or 5, wherein for transfer from mains mode to back-up mode, said mode transfer control unit comprises:

means for generating a disabling signal for said transfer control switch, said battery charger and said power factor corrector;

means for turning off said first, third and fourth control signals for said transfer switch, said battery charger and said power factor corrector after reception of said disabling signal;

means for generating an enabling signal for said inverter, said battery voltage booster and said power factor corrector filter, after said first, third and fourth signals were turned off; and

means for turning on said second and fifth control signals for said inverter, said battery voltage booster

and said power factor corrector filter, after reception of said enabling signal.

8. A system as claimed in claim 1 or 5, wherein for transfer from said back-up mode to said mains mode, said mode transfer control unit comprises:

means for generating a disabling signal for said inverter, said battery voltage booster and said power factor corrector filter;

means for turning off said second and fifth control signals for said inverter, said battery voltage booster and said power factor corrector filter after reception of said disabling signal;

means for generating an enabling signal for said transfer control switch, said battery charger and said power factor corrector, after said second and fifth control signals were turned off; and

means for turning on said first, third and fourth control signals for said transfer control switch, said battery charger and said power factor corrector, after reception of said enabling signal.

9. A system as claimed in claim 1 or 5, wherein said transfer switch is formed with a pair of unidirectional static switches connected back-to-back, said static switches being gate controlled with said first control signal.

10. A system as claimed in claim 1 or 5, wherein said control unit includes circuits for controlling said switching elements of said inverter bridge, comprising:

means for sensing the voltage and current of said inverted AC signal;

means for generating a reference waveform with a target nominal frequency and voltage;

means for comparing said sensed inverted AC signal and said reference waveform and giving a difference

signal;

Kalman filter means for receiving said difference signal and generating an output which traces the sensed inverted AC signal with zero steady-state error, for assessing an estimated voltage value of said sensed inverted AC signal;

means for determining the root-mean-square voltage of said output and comparing it with a preset reference to generate an error signal;

a PI loop control for processing said error signal to obtain a modulating signal;

a PWM generator for comparing said modulating signal with a triangular carrier wave to obtain a positive high frequency PWM signal for a first and a fourth switching element and a negative high frequency PWM signal for a second and a third switching element and applying gate control signals for controlling said high frequency switching elements of said inverter bridge.

11. A system as claimed in claim 3 or 5, wherein said battery voltage booster is a DC-DC converter which regulates said unregulated battery voltage to said third DC signal at the input of said inverter comprising:

a first inductor series connected to said battery node;

a first switching element connected between said inductor and common node, controlled with said fifth control signal to turn on for applying said battery voltage to said first inductor for charging it and to turn off for allowing discharge of the electrical energy from said first inductor into said inverter;

a series connected first diode for ensuring that said third DC signal is greater than said battery voltage; and

a first DC capacitor connected to said second node for filtering said third DC signal.

12. A system as claimed in claim 11, wherein said control unit includes circuits for controlling said first switching element of said battery voltage booster comprising:

means for sensing said third DC signal;

means for comparing said sensed third DC voltage with a reference voltage and generating an error signal;

a PI loop control for processing said error signal to obtain a modulating signal;

A PWM generator for comparing said modulating signal with a triangular carrier wave for obtaining said fifth control signal; and

means for adjusting said reference voltage for limiting the current of said third DC signal below a safety limit.

13. A system as claimed in claim 6, wherein said power factor corrector is a boost DC-DC converter based power factor correction network comprising:

a second inductor series connected to said first node;

a second switching element connected to said second inductor and to the common node, controlled with said third control signal to turn on for applying to said second inductor said first DC signal for charging it, and is turned off for allowing discharge of the electrical energy from said second inductor to said battery charger;

a second diode series connected between said second inductor and said second node for ensuring that said second DC signal voltage is greater than said first DC signal voltage; and

a first DC capacitor connected to said second node for filtering said second DC signal.

14. A system as claimed in claim 13, wherein said control unit include circuits for controlling said second switching element of said power factor corrector,

comprising:

means for generating a sliced rectified sinewave using said states variables for obtaining a modulating signal;

means for sensing the voltage of said second DC signal and comparing it with a PFC reference voltage to obtain a difference signal;

means for adjusting said modulating signal using said difference signal and adjusting said weighting factors; and

a PWM generator for comparing said modulating signal with a triangular carrier wave to obtain said third control signal with a phase shift ϕ and an amplitude α determined by said state variables ϕ.

15. A system as claimed in claim 2 or 5, wherein said battery charger is a buck DC-DC converter comprising:

a first inductor series connected to said battery node;

a third diode connected between said first inductor and the common node;

a third switching element series connected between said first inductor and said second node, controlled with said fourth control signal to turn on for charging said first inductor with said second DC signal and to turn off for discharging the energy from said first inductor into said battery node through said second diode; and

a second DC capacitor connected in parallel to said battery node for obtaining a smooth battery charge voltage.

16. A system as claimed in claim 15, wherein said control unit includes circuits for controlling said third switching element of said battery charger, comprising:

means for sensing the voltage and the current of said battery signal;

means for generating a battery reference voltage;

means for comparing said sensed voltage with said battery reference voltage;

a PI loop control for processing said difference signal and giving a modulating signal;

a PWM generator for comparing said modulating signal with a triangular carrier wave to obtain said fourth control signal;

means for adjusting said modulating signal with for limiting the current of said battery charging signal below a safety limit.

17. A system according to any of the preceding claims, wherein the battery charging voltage is regulated at 165 VDC.

18. A system according to any of the preceding claims, wherein the AC mains supplies the battery charging power with the power factor maintained above 0.9.

19. A single phase off-line uninterruptable power supply system constructed and arranged to operate substantially as hereinbefore described with reference to and as illustrated in the accompanying drawings.

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Patents Act 1977 **Examiner's report to the Comptroller under Section 17** **(· Search report)**	Application number GB 9407933.2
Relevant Technical Fields (i) UK Cl (Ed.M) H2H HAJ (ii) Int Cl (Ed.5) G05F 1/70; H02J 9/00, 9/04, 9/06; H02M 1/00	Search Examiner M J BILLING Date of completion of Search 7 JUNE 1994
Databases (see below) (i) UK Patent Office collections of GB, EP, WO and US patent specifications. (ii) ONLINE DATABASE: WPI	Documents considered relevant following a search in respect of Claims :- 1-5

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Category	Identity of document and relevant passages		Relevant to claim(s)
X,Y	GB 2210214 A	(CHLORIDE) eg see elements 26, 27, 61, 72-75 in Figure 1	X:1 at least Y:2
X,Y	GB 2171861 A	(EXIDE) eg see elements 44, 46, 48, 78 in Figure 11	X:1 at least Y:2
X,Y	US 5221862	(MERLIN GERIN) eg see Figure 1; column 3 lines 24-53	X:1 at least Y:2
X,Y	US 5172009	(MOHAN) eg see elements 32, 35, 42, 84 in Figure 1; abstract	X:1 at least Y:2
X,Y	US 4827151	(TOSHIBA) eg see common circuit 5 in Figure 1; column 5 lines 7-23	X:1 at least Y:2
X,Y	US 4065711	(MITSUBISHI) eg see elements 8, 18, 21 in Figure 3	X:1 at least Y:2
Y	S Sivakumar, K Natarajan, "Kalman filter based high speed measurement and control of AC voltages for UPS application", 1993 IEEE. Power Electronics Specialists Conference Record pages 907-912, Seattle, Washington June 1993 - especially page 910 parts 6 and 11		

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